Multi-Gigabit Low-Power Wireless CMOS Demodulator

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Multi-Gigabit Low-Power Wireless CMOS Demodulator

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To the Loving Memories of My Mom

To My Always Supportive Dad

To My Loving & Caring Wife

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Summary

With demanding requirements of ever-increasing data storage and multi-media intensive content, the next-generation wireless communication system has to accommodate multi-gigabit applications such as data transfer and HD video streaming. However, the traditional transceiver architecture with power-hungry data–converters and DSP modems limits the portability of the device operating at such high-speed. In order to incorporate this functionality in a more versatile, reliable and affordable way, alternative system architectures are investigated to achiever low-power multi-gigabit demodulation in CMOS technologies. With the availability of wideband spectra, both UWB and millimeter-wave frequency bands (60 GHz, 70 GHz, 80 GHz and 90 GHz) provide the perfect vehicles to bring the ultra-portable multi-gigabit WPAN and WLAN applications into reality.

This dissertation presents system and circuit development of the low-power multi-gigabit CMOS demodulator using analog and mixed demodulation techniques. In addition, critical building blocks of the low-power analog quadrature front-ends are designed and implemented using 90 nm CMOS with a targeted compatibility to the traditional demodulator architecture. It exhibits an IF-to-baseband conversion gain of 25 dB with 1.8 GHz of baseband bandwidth and a dynamic range of 23 dB while consuming only 46 mW from a 1 V supply voltage. Several different demodulators using analog signal processor (ASP) are implemented: (1) an ultra-low power non-coherent ASK demodulator is measured to demodulate a maximum speed of 3 Gbps while consuming 32 mW from 1.8 V supply; (2) a mere addition of 7.5 mW to the aforementioned analog

quadrature front-end enables a maximum speed of 2.5 Gbps non-coherent ASK demodulation with an improved minimum sensitivity of -38 dBm; (3) a robust coherent BPSK demodulator is shown to achieve a maximum speed of 3.5 Gbps based on the same analog quadrature front-end with only additional 7 mW. Furthermore, an innovative seamless handover mechanism between ASP and PLL is designed and implemented to improve the frequency acquisition time of the coherent BPSK demodulator. These demodulator designs have been proven to be feasible and are integrated in a 60 GHz wireless receiver. The system has been realized in a product prototype and used to stream HD video as well as transfer large multi-media files at multi-gigabit speed.

Chapter I

Introduction

1.1 Motivation

Over the past two decades, the technology evolution of the wireless industry has dramatically changed everyone's lifestyle. From the simple need of voice services to the ubiquitous Internet access with soaring multi-media content, the ever-expanding demand of the consumers has driven the development of higher speed, multi-functional, better portability and lower cost wireless devices. These challenging requirements force higher chip-level and package-level integration of multiple co-existing wireless standards while maintaining a low-power and reliable communication.

The coverage, throughput and network topology of any wireless standard are determined by its targeting applications. Figure 1-1 shows a comparison chart of coverage versus data speeds for various established and developing wireless standards intended for consumer applications. The legacy 2G cellular phone systems, namely advanced mobile phone system (AMPS), digital-AMPS (D-AMPS), global system for mobile communication (GSM), and code division multiple access (CDMA), provide suitable platforms for the voice and low data rate services (such as text messaging) up to a few Kbps. By combining multiple data channels in either frequency or time domains, the 2.5G technologies such as general packet radio services (GPRS), enhanced data rates

for global vvolution (EDGE) and CDMA2000, made applications that require hundreds of Kbps into reality. Examples are text-based Internet browsing, email access and multi-media file exchange. However, the wireless data speed needs to be further boosted due to the ever-increasing sizes of web pages. Hence 3G services like universal mobile telecommunication system (UMTS), high-speed downlink packet access (HSDPA) and evolution-data optimized (EVDO) offer a few Mbps of data speed, which rivals the traditional cable and digital subscriber line (DSL) services. These cellular-based networks can cover subscribers within miles of the base station (BS) without line-of-sight.

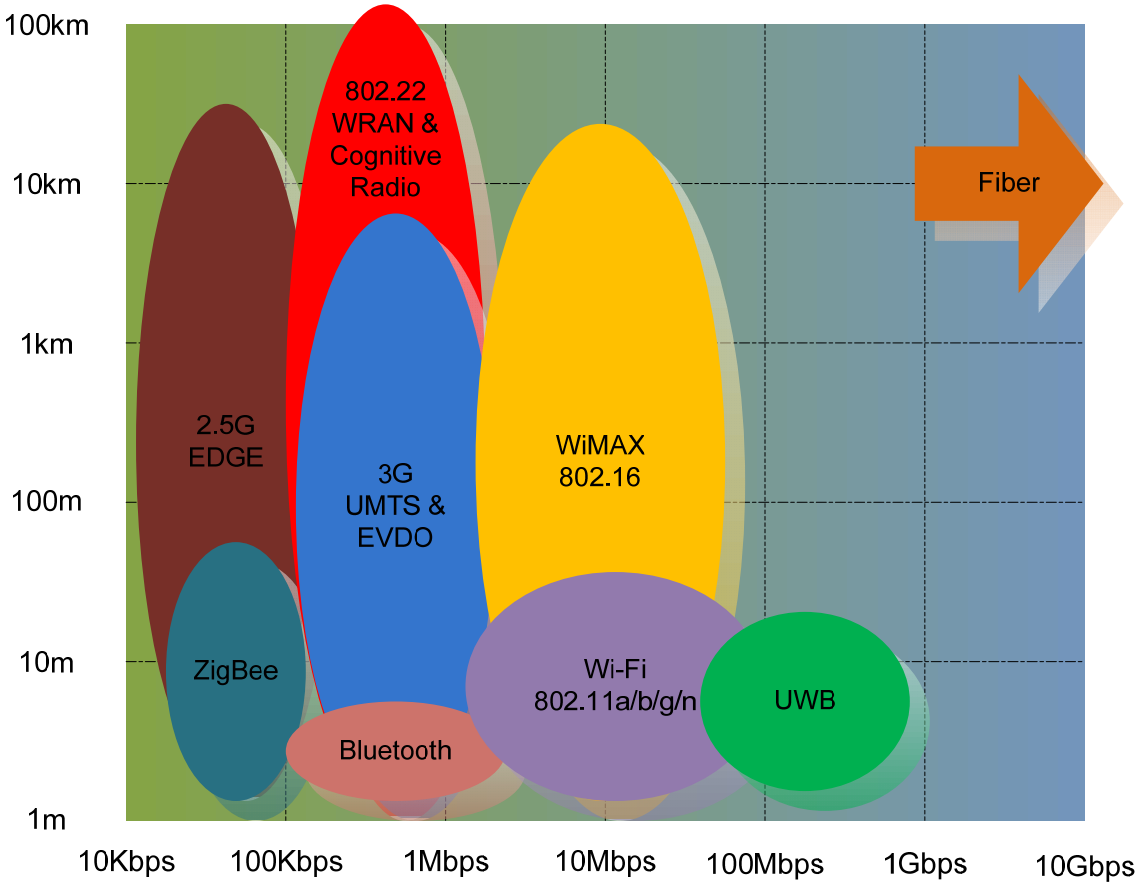


Figure 1-1: Coverage versus data speed for various **w**ireless standards [1]

In contrast, the popular Wi-Fi, IEEE802.11a/b/g/n wireless local area network (WLAN) standards satisfy the requirements of a relatively smaller coverage (more than 50 feet away from the access point) and higher speed (a 100 Mbps with multiple-input and multiple-output (MIMO)) applications such as hot-spots, campus-wide and home wireless networking. The upcoming worldwide interoperability for microwave access (WiMAX) standard is a cross-breed between cellular and WLAN technologies, in which a cellular-type network providing similar or higher data speed than WLAN. It has sometimes been marketed as the 4G service by the some cellular service providers. WiMAX provides a fixed broadband solution (almost 100 Mbps) as the last-mile alternative to DSL cable modem in a rural area. At the same time, it could also serve as the mobile (in-vehicle) broadband option in metropolitan areas at slightly lower data rates.

The wireless personal area network (WPAN) standards (e.g. Bluetooth and ZigBee) offer a low-power and low-cost alternative to its wired counterpart (usually used as the short-distance cable replacement). It provides up to a few Mbps of data communication using a simple ad-hoc network connection. The short range (e.g. less than 30 feet) feature makes the WPAN devices suitable for low-cost, secure and ultra-portable wireless interconnection between laptops, cellular phones, PDA's, digital cameras and GPS devices.

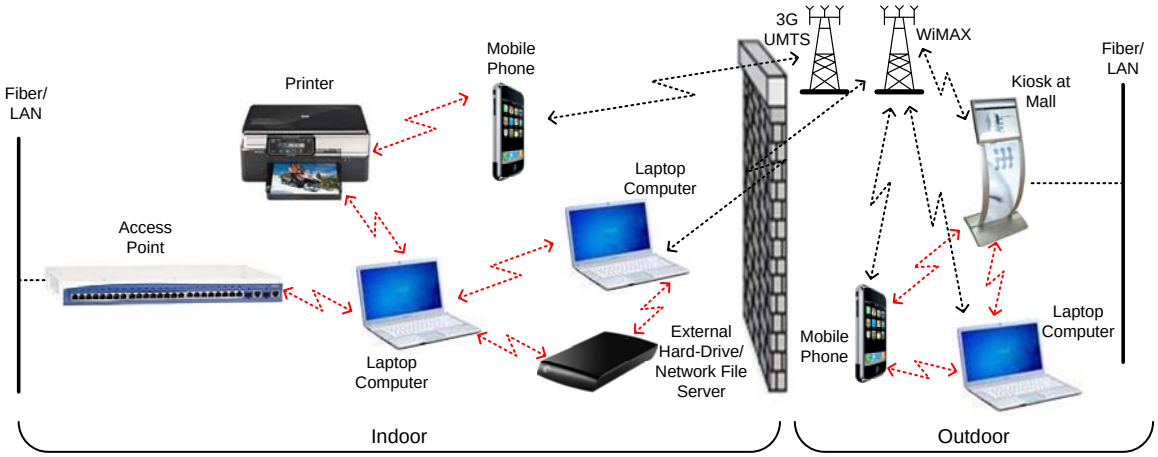
The maximum achievable data speed of these aforementioned wireless technologies and standards is hundreds of Mbps and it is not sufficient for future commercial, industrial and military applications in the multi-gigabit range. In order to accommodate the upcoming multi-gigabit wireless applications such as short-range high definition (HD)

multi-media exchange, point-to-point digital backhaul radio trunk and high-bandwidth download kiosk, scientists and researchers are exploring new communication systems and architectures to address the requirements of these devices, which are low-cost, portability and integration with existing user platforms. Currently, ultra-wideband (UWB) is a high-speed short range WPAN technology that has demonstrated capability of raw wireless throughputs close to 500 Mbps [2] [3].

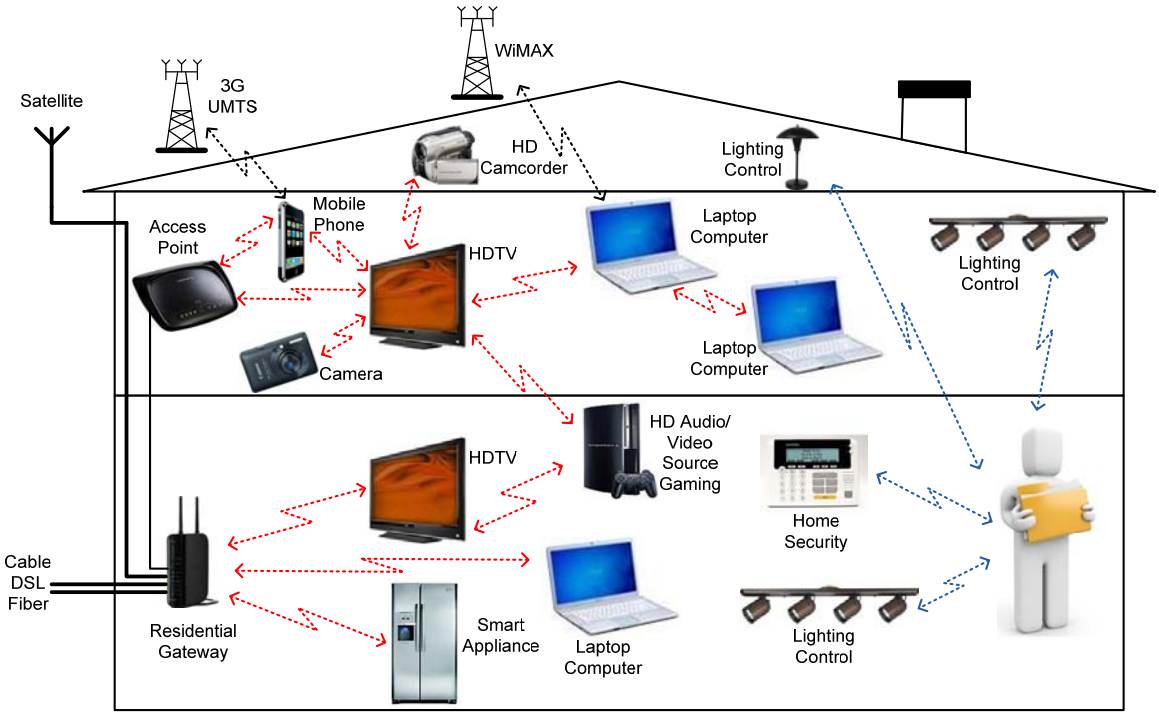
Figure 1-2(a) and (b) show examples of the potential multi-gigabit consumer applications in an indoor office, outdoor/mobile and home environments although commercial and industrial users can also benefit from this upgrade of data speed [4]. The red line indicates potential applications of the multi-gigabit data communication and they can coexist with the established cellular-based services (3G and WiMAX) as shown in black lines as well as the lower data-rate links shown in blue. These multi-gigabit data links cannot be realized by today's technologies. At its best, the consumers have to settle for Wi-Fi type of speed (less than 100 Mbps). However, demands for high-definition multi-media content (e.g. 1080p or higher video) and large data-storage (e.g. 3 TeraBytes for personal external hard-drives) are expected to grow at a much faster pace that a wireless multi-gigabit data transmission is no longer a high-end luxury product feature but a must [5].

Among all potential multi-gigabit applications, portable and mobile battery-operated devices present the largest technology huddle due to its ultra low-power constraints. This is not to discount other technical issues that also are needed to be addressed in order to bring the wireless multi-gigabit data transmission into reality. Given

these challenges, which are elaborated later, a convergent top-down system approach is necessary for a low-power multi-gigabit implementation.



(a)



(b)

Figure 1-2: Examples multi-gigabit applications for (a) indoor office and outdoor/mobile environments; (b) home and small-office environments

1.2 Challenges

From wireless media access control (MAC) protocols, packaging, transceiver system, modulation schemes to circuit implementation, different technical issues and obstacles come into play when designing a multi-gigabit wireless communication system. According to the Shannon's Information Capacity Theorem [6], the theoretical throughput of any communication system is limited by the following formula

$$C = BW \times \log_2(1 + SNR) \tag{1}$$

where, C (in bits per second) is the maximum data speed of the system, BW is the continuous channel bandwidth, and SNR is the received signal-to-noise ratio (in linear form). The theorem implies that data transmission with arbitrarily small bit error rates can be achieved by using a power-limited and bandwidth-limited additive white Gaussian noise wireless channel. Since this fundamental speed limit, C is linearly related of the channel bandwidth and logarithmically dependent of the signal-to-noise ratio, it is simpler to boost the information capacity of a communication system by increasing its channel bandwidth instead of raising the transmitted power to obtain a higher SNR. It means that, 1 Gbps wireless transmission can be achieved through either 1 GHz of bandwidth using 1-bit/Hz modulation or 125 MHz of bandwidth using 8-bits/Hz modulation. However, 8-bit/Hz modulation generally requires a much higher SNR (e.g. 34 dB of SNR is required for a 256-QAM at BER=1×10^{-8}) in order to be demodulated correctly and this means a more stringent signal-integrity and noise specifications for the wireless receiver and higher power and linearity requirements for the transmitter. This

would result in higher power consumption and, making it difficult to have a multi-gigabit wireless solution integrated into mobile applications. In addition, over the last decade, Federal Communications Commission (FCC) has re-evaluated the utilization of its governed wireless spectrum and has since re-allocated multiple formally unused or underutilized wideband spectra, e.g. 3.1~10.6 GHz, 22~29 GHz, 60 GHz, 70 GHz, 80 GHz, 90 GHz and the previously occupied analog TV broadcast spectrum [7]. These newly vacant spectra provide the perfect vehicles for a multi-gigabit wireless system to be used in a variety of scenarios depending on the target applications.

With the wideband spectra available, another critical technical issue is the multi-gigabit demodulator design for the wireless transceiver. Figure 1-3 shows a typical architecture that has been widely implemented in the almost all narrowband transceivers on the markets, e.g. Wi-Fi, WiMAX devices and cell phones. It allows the DSP modem to perform numerous complex operations such as equalization and error-correction in the digital domain. However, this architecture is limited to sub-100 Mbps transmission speed and it is not scalable to the mobile multi-gigabit wireless system due to the power hungry analog-to-digital converters (ADC) and high-speed modem. These Nyquist-rate ADCs has a minimum sampling frequency of several gigahertzes in order for the DSP to demodulate the down-converted baseband signal. The power consumption of an ADC increases rapidly with either higher sampling speed or additional bit of resolution [8]. In addition, the DSP also has to function at a speed in the same order of the magnitude as the ADC sampling speed, i.e. in GHz. Such high speed signal manipulation would draw a significant amount of current. As a reference point, one state-of-art 6-bit 3.5 GHz CMOS ADC consumes close to 100 mW [9]. This implies that the overall power budget for the

physical layer of the multi-gigabit transceiver would be close to 1 W after considering the power consumption of the RF front-end and DSP modem. Therefore, it is important to find alternatives to digital high-speed demodulation technique and one option is to move this function into the analog domain.

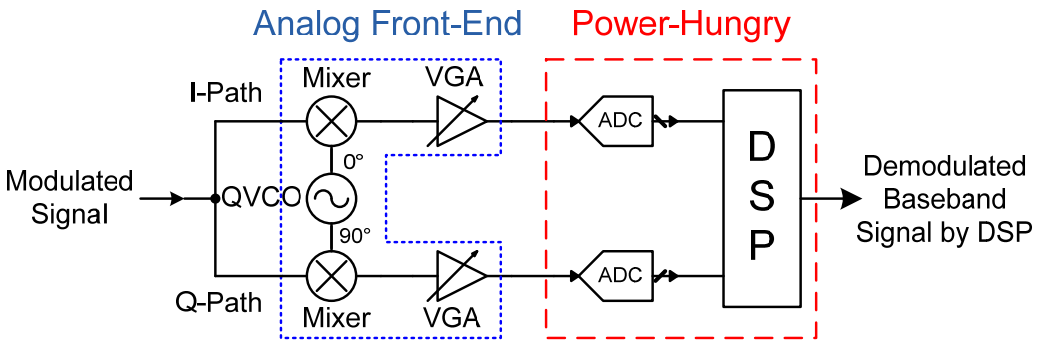


Figure 1-3: Typical demodulator architecture

The object of this research is to explore the system development of a multi-gigabit low-power wireless complementary metal-oxide semiconductor (CMOS) demodulator integrated circuits (IC) for the next generation multi-gigabit receiver chipset for mobile battery-operated devices. Non-traditional analog demodulation solutions are chosen over the popular ADC approach due to the aforementioned stringent power-budget for the portability purpose.

1.3 Organization of Dissertation

The dissertation is organized as followed. The second chapter provides a brief overview of the wireless multi-gigabit system. Top-level issues such as modulation schemes and receiver architectures are evaluated and their respective performance is assessed in terms of throughputs, minimum sensitivity, power consumption, size and robustness. In addition, a summary of current technologies in UWB and millimeter-wave frequencies is given to show the potentials of a wireless multi-gigabit system in the near future. The link budget is also examined in the second chapter to complete the overall system analysis.

The third chapter presents the circuit and system development of the analog quadrature front-end for the multi-gigabit demodulator using 90 nm CMOS processes. Mixers, quadrature voltage-controlled oscillator (QVCO) and baseband variable gain amplifiers (VGA) with automatic gain-control (AGC) mechanism are the essential functional blocks of the analog front-end. These building blocks are initially implemented using 1.8 V power supply to demonstrate its feasibility. However, a low-voltage version of these circuits is also implemented for 1 V supply operation to further reduce the power consumption of the analog front-end. In addition, several broadband techniques are applied in the VGA design to maintain high-gain and high bandwidth in the baseband signal path. Finally, an integrated analog quadrature front-end demonstrates a conversion gain of 25 dB with 1.8 GHz of baseband bandwidth and a dynamic range of 23 dB while consuming 46 mW from a 1 V supply.

The fourth chapter introduces two distinct non-coherent low-power multi-gigabit CMOS ASK demodulator architectures using analog signal processing techniques. The former is based on the frequency discriminator design and it is shown to be capable of more than 3 Gbps ASK demodulation at merely 32 mW power consumption (10.67 pJ/bit). The later utilizes the aforementioned analog front-end with a compact integrated ASK demodulator, which is an innovative re-use of the power detector circuit inside the AGC to perform the I^2+Q^2 operation. Hence, this design is compatible with the traditional digital modem approach (if desired) and simultaneously provides more than 2.5 Gbps ASK demodulation speed with a better sensitivity of -38 dBm at only an additional 7.5 mW DC power consumption (3 pJ/bit).

The fifth chapter presents a multi-gigabit low-power coherent BPSK demodulator solution using analog signal processor and its design is also compatible with the traditional digital modem approach. It is demonstrated in this dissertation that the multi-gigabit system is capable of reaching a maximum speed of 3.5 Gbps demodulation with a minimum sensitivity of -47 dBm (at 1.782 Gbps) at only 7 mW additional DC power consumption. Furthermore, wireless HD streaming experiments are performed to validate its functionality and capability. In addition, a sophisticated automatic hand-over mechanism between the analog signal processor and the integrated phase-locked loop is implemented to improve the overall system robustness against any carrier frequency drift and process, temperature variations.

Finally, the unique contributions of this research and the related future works are summarized in the sixth chapter.

Chapter II

Overview of Multi-Gigabit System

2.1 Introduction

This chapter revisits the multi-gigabit system from the top-level system issues to the IC fabrication process. At the beginning, an overview of the current technologies in UWB and millimeter-wave frequency bands is provided to show the potential applications of the multi-gigabit system in the near-future. Both heterodyne and direct-conversion receiver architectures are discussed in relation to the multi-gigabit demodulator design. Amplitude, phase and frequency modulation schemes are compared in terms of their power and spectrum efficiencies. In addition, traditional single and multi-carrier demodulation techniques using DSP are presented to further illustrate the importance of low-power analog signal processor in the next-generation multi-gigabit demodulator. A brief review of the CMOS IC process is given and the critical role of technology scaling is emphasized. Finally, the link budget analysis is also performed to illustrate the trade-off between coverage and data speed.

2.2 Overview of Current Technologies

2.2.1 Ultra-Wide Band

In February 2002, FCC officially authorized the contiguous frequency spectrum of 3.1~10.6 GHz to be used for UWB technology in United States (see Figure 2-1(a)). However, the FCC regulation limits the emitted power spectral density of -41.3 dBm/MHz (based on an isotropic transmit antenna) for outdoor use of the UWB system (see Figure 2-1(b)) [10]. Additionally, the transmitted signal spectrum must occupy an instantaneous operating bandwidth of either 500 MHz or more than 20% of its center frequency. The wideband requirement and power restrictions of such UWB links ensures interference-free wireless channels for the existing narrowband in-band technologies (Wi-Fi IEEE 802.11a, unlicensed national information infrastructure (U-NII), proprietary licensed radar, satellite, microwave backhaul and military applications). This causes the UWB signal to be closer to the noise level in those unintended receivers. Nevertheless, UWB provides the potentials of a low-cost high-speed PAN connectivity and short-range docking. Internationally, different frequency bands are also proposed for UWB operations by the regulatory bodies in Europe (6.0~8.5 GHz and 3.5~4.5 GHz with detect and avoid (DAA)) and Japan (3.4~4.8 GHz and 7.25~10.25 GHz).

Currently there are two competing proposing PHY-standards for UWB technologies: one is the multi-band OFDM alliance (MBOA) supported by WiMedia and the other is the direct-sequence UWB (DS-UWB) supported by UWB Forum [11]. Both standards exhibit competitive features and advantages of their own as the MBOA is based

on the popular success of the WLAN 802.11 technology and the DS-UWB utilizes a short-impulse radio (i.e. wideband) spread spectrum technology similar to the CDMA operation. However, neither proposal gains substantial industrial momentum even with the support of major IC chip players. In addition, the lack of standardization progress impedes the full-fledge business development of the UWB technology [12]. With the emergence of license-free 60 GHz millimeter-wave technology (to be discussed later) providing potentially higher data rates, the future outlook of the UWB technology seems gloomy.

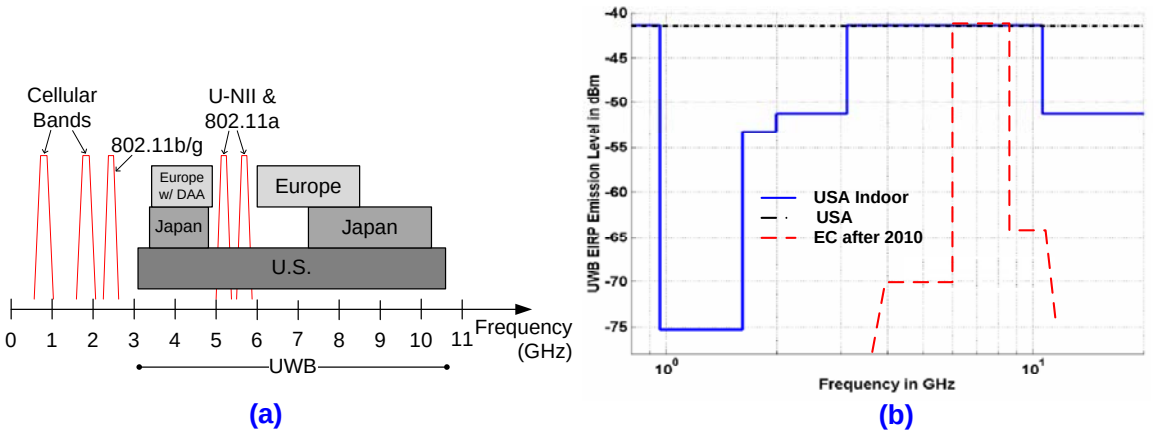


Figure 2-1: (a) Frequency allocation of UWB throughout the world; (b) emission spectrum mask

2.2.2 Millimeter-Wave

Traditionally, the millimeter-wave frequency spectrum (30~300 GHz), sometimes called extremely high frequency (EHF), is for the exclusive usage of military, government and astronomy applications [13]. However, with the availability of advanced technologies and promoting of ever-growing telecommunication industries in mind, in

2001, FCC set aside a continuous block spectrum of 7 GHz between 57~64 GHz for license-free operation in United States (see Figure 2-2(a)). Shortly after that, in October 2003, previously unused spectrum of 71~76 GHz, 81~86 GHz and 92~95 GHz are also allocated by FCC for high-density fixed wireless services [14]. These unprecedented rulings have opened up opportunities to the research and development of millimeter-wave wireless electronics. The rules also provided one critical factor that was previously not available in the traditional narrowband radios, namely GHz of bandwidth. As discussed in Section 1.2, the availability of wide bandwidth is the main catalyst of the next generation low-power multi-gigabit system.

The frequency spectrum around 60 GHz (as well as 24 GHz) is part of the so-called oxygen absorption band, in which significant attenuation by the oxygen molecules compounded with huge free-space path loss hinders the coverage (within 30 feet) of any wireless system operating in that band. This can be seen as a peak of the sea level attenuation in Figure 2-2(a) and high rain-attenuation in Figure 2-2(b) at 60 GHz. On the other hand, the same attribute results in reduced multi-path effects as well as enables a secure communication channel (almost impossible to eavesdrop) and higher frequency-reuse, i.e. more 60 GHz wireless devices can operate simultaneously without interfering with each other [15]. Throughout the world, different standard bodies, such as ECMA, IEEE802.15TG3c, WirelessHD and Wireless Gigabit Alliance (Wi-Gig), are all searching for diverse prospective applications to utilize this license-free wide spectrum.

On the other hand, the potential technologies at frequency spectrum of 70 GHz, 80 GHz and 90 GHz only need to compete with the rain fading factor without the extra loss

due to the oxygen-absorption. This can be seen as a small window of low sea level attenuation in Figure 2-2(a) before the next peak shows up at approximately 110 GHz. Hence, they are perfect candidates for carrier-class commercial multi-gigabit digital link backhaul applications as optical fiber replacement or extension. A link distance of several miles is achievable with propagation characteristics being slightly worse than the commercially available microwave link products. This results in low-cost, high-reliability multi-gigabit system. In this research dissertation, the license-free 60 GHz is chosen to be the millimeter-wave example for the proposed multi-gigabit demodulator.

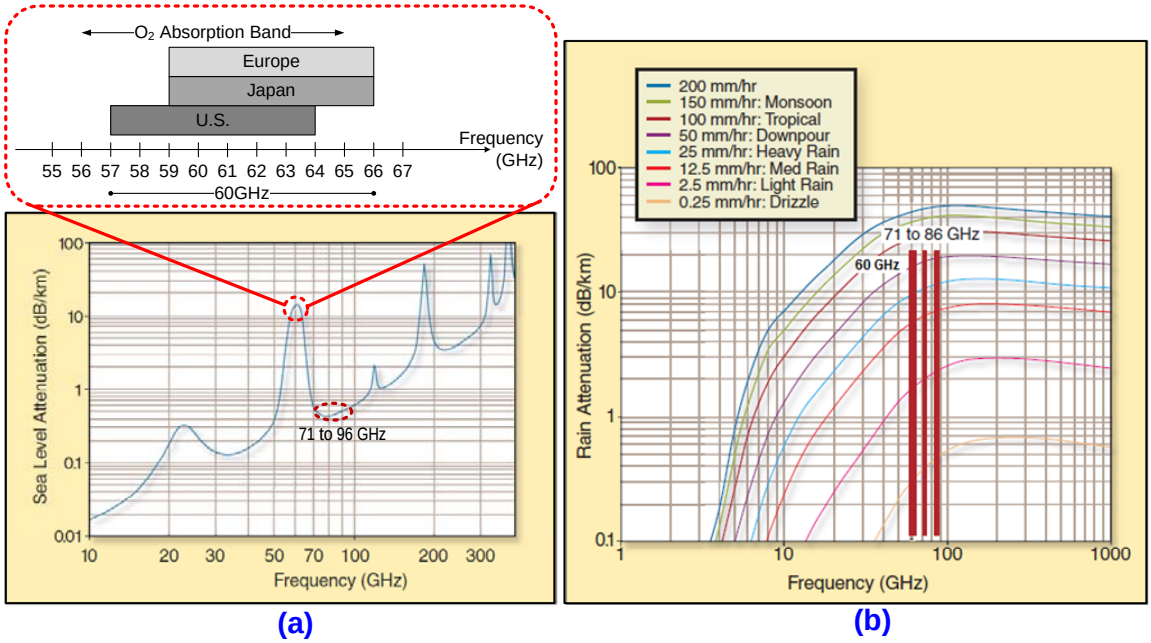


Figure 2-2: (a) Sea level attenuation of millimeter-frequency signal spectrum and the frequency allocation of 60 GHz technologies throughout the world; (b) rain attenuation vs. millimeter-wave signals [14]

2.3 Receiver Architectures

Based on the chosen technology, UWB or millimeter-wave, two receiver architectures are possible for the implementation of the multi-gigabit demodulator and the architectures are shown in Figure 2-3. For the millimeter-wave (mmW) receiver, the super-heterodyne architecture is employed with the RF front-end (at 60 GHz, 70 GHz, 80 GHz or 90 GHz) first down-converting the RF signal to intermediate frequency (IF), in which the IF mixer and voltage-controlled oscillator (VCO) handles the second down-conversion to the baseband signal. On the other hand, the direct-conversion architecture is used in the UWB system, in which the low-noise amplifier (LNA) followed by the mixer directly down-converts the received signal from UWB band to baseband.

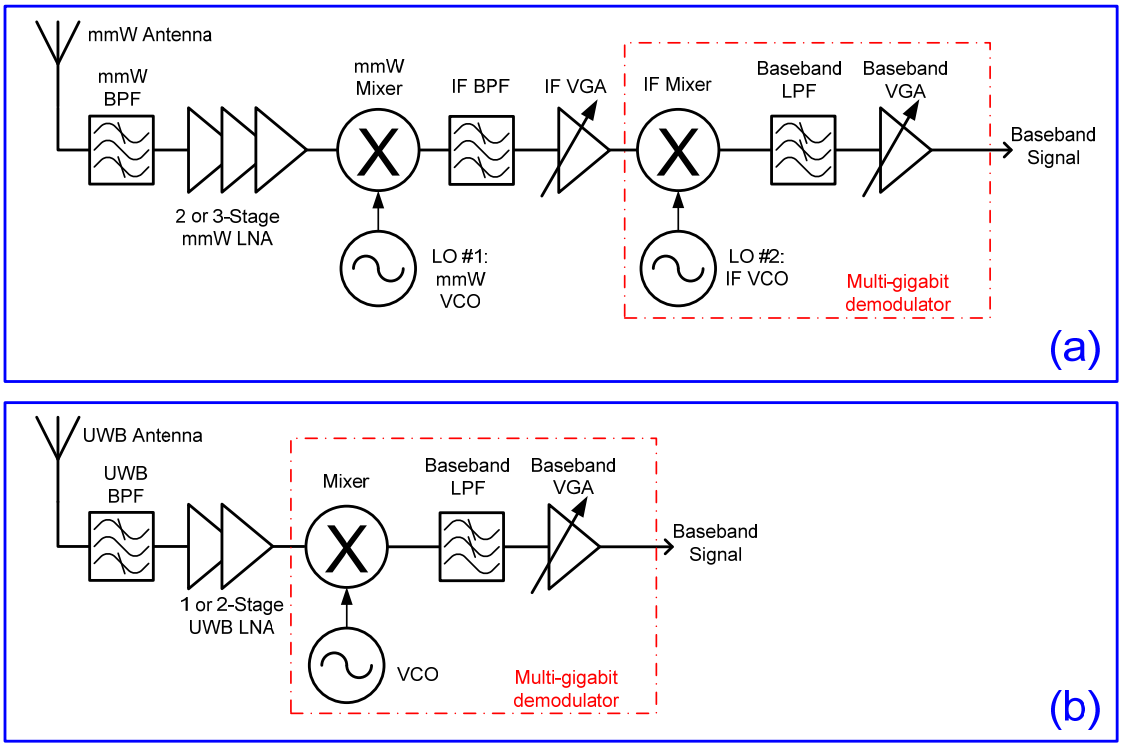


Figure 2-3: Receiver architectures for the multi-gigabit demodulator: (a) super-heterodyne for millimeter-wave system; (b) direct-conversion for UWB system

The circled portion in Figure 2-3 is the same in both architectures. It implies a re-use of the UWB's multi-gigabit demodulator in the millimeter-wave receiver is possible if the oscillation frequency (f_{mmW}-f_{IF}) of the mmW VCO is carefully chosen such that IF overlaps the UWB frequency band. However, the IF in the super-heterodyne architecture can also be selected based on the overall frequency planning of the transceiver. Although the multi-gigabit demodulator (shown in Figure 2-3) constitutes of a mixer, a VCO, a low-pass-filter (LPF) and a VGA, a power-detector based (without VCO) demodulator can also be employed. In this case, the modulated signal is sensed directly at the UWB or other IF frequencies. The down-converted baseband signal is then sampled by the ADCs, where the digital signal processing begins and this is discussed in details in the next section.

2.4 Digital Modulation Schemes

Digital modulation can be achieved by varying one or more properties of the RF carrier: amplitude, frequency and phase. Binary amplitude shift keying (ASK) is the simplest and most commonly used modulation scheme in the communication system because of its inexpensive and straightforward modulation and demodulation implementation. ASK transmits logic 1's and 0's using the traditional analog amplitude modulation (AM). Hence, the information is being sent by modulating the amplitude of the carrier and it appears as the envelope of the transmitted signal waveform. On-off keying (OOK) is a special case of ASK, in which nothing or null is transmitted with a

logic 0. The ASK-modulated waveform can be represented in the following mathematical form

$$R_{ASK}(t) = D(t) \times \cos(\omega_{ASK} t), \text{ where } D(t)=A \text{ for 1; null for 0 in OOK} \quad (2)$$

where, ω_{ASK} is the oscillator carrier frequency and *D(t)* is the modulating baseband digital signal. The signal space of an ASK signal is depicted in Figure 2-4(a). Binary frequency shift keying (FSK) and its variants have been employed in a variety of applications such as remote-metering and sensing. GSM cellular standards utilizes one special type of FSK modulation, called Gaussian minimum shift keying (GMSK) in which logic 1's and 0's are transmitted as two orthogonal bases in the signal space as shown in Figure 2-4(b). The FSK-modulated waveform can be represented in the following mathematical form

$$R_{FSK}(t) = A_C \cos\left\{\left[\omega_C + \frac{1}{2} D(t)\Delta\omega\right]t\right\}, \text{ where } D(t)=1 \text{ or } -1 \quad (3)$$

where, A_C is the constant carrier amplitude and "$\omega_C+0.5\Delta\omega$" *and* "$\omega_C-0.5\Delta\omega$" are the two distinct instantaneous carrier frequencies being transmitted. Binary and quadrature PSK are the two most popular digital modulation schemes being deployed in today's data-centric wired and wireless communication networks. From a few Kbps to more than several hundreds of Mbps data speeds, PSK and its variants found its use almost everywhere from Bluetooth to satellite links. As BPSK utilizes the phase (0º and 180º, i.e. polarity) of one single carrier to transmit/receive the digital data stream, QPSK doubles its data speed with one additional orthogonal carrier as shown in the signal spaces (Figure 2-4(c) and Figure 2-4(d)). The BPSK- and QPSK-modulated waveforms can be represented in the following mathematical form

$$R_{BPSK}(t) = D(t)\cos(\omega_{BPSK}t), \text{ where } D(t)=A \text{ for1; } -A \text{ for } 0 \quad (4)$$

$$R_{QPSK}(t) = D_I(t)\cos(\omega_{QPSK}t) + D_Q(t)\sin(\omega_{QPSK}t),$$

$$\text{where } D_I(t) \text{ and } D_Q(t)=A/\sqrt{2} \text{ for1; } -A/\sqrt{2} \text{ for } 0 \quad (5)$$

where, $D_I(t)$ and $D_Q(t)$ are the two separate data streams used to modulate the two orthogonal carriers, $cos(\omega_{QPSK}t)$ and $sin(\omega_{QPSK}t)$, individually. To increase the data speed even further without using additional bandwidth, higher-level QAM (more bits per symbol) can be achieved by applying more than binary ASK modulation to the two individual orthogonal carriers, such as 4-level ASK for 16-QAM, 8-level ASK for 64-QAM and 16-level for 256-QAM. However, as discussed earlier, higher-level modulation requires much higher SNR in order to be demodulated correctly and it is more difficult to perform all required signal processing operations for the multi-gigabit demodulator without going over the power budget. Hence, binary ASK, binary FSK, BPSK and QPSK are the primary candidates for the physical implementation of the multi-gigabit system.

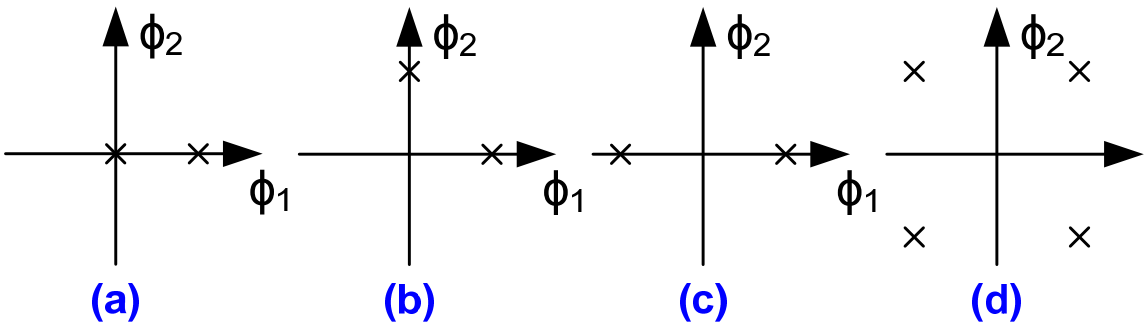


Figure 2-4: Signal space of (a) binary ASK signal; (b) binary FSK signal; (c) binary PSK signal; and (d) quadrature PSK signal

A brief comparison of the theoretical probability of error, bandwidth and power efficiency between different binary modulation methods are shown in Table 2-1 [16]. The theoretical probability of error under different received SNR values for binary ASK, FSK and PSK are plotted in Figure 2-5**:** Probability of error versus signal-to-noise ratio , in which *erfc(•)* represents the complementary error function.

Table 2-1: Performance comparison of binary ASK, FSK and PSK modulation schemes

	ASK	**FSK**	**PSK**
Theoretical probability of error vs. SNR	$\frac{1}{2}erfc(\frac{\sqrt{SNR}}{2})$	$\frac{1}{2}erfc(\sqrt{\frac{SNR}{2}})$	$\frac{1}{2}erfc(\sqrt{SNR})$
Bandwidth Efficiency	Good	Poor	Good
Power Efficiency	Poor	Good	Good

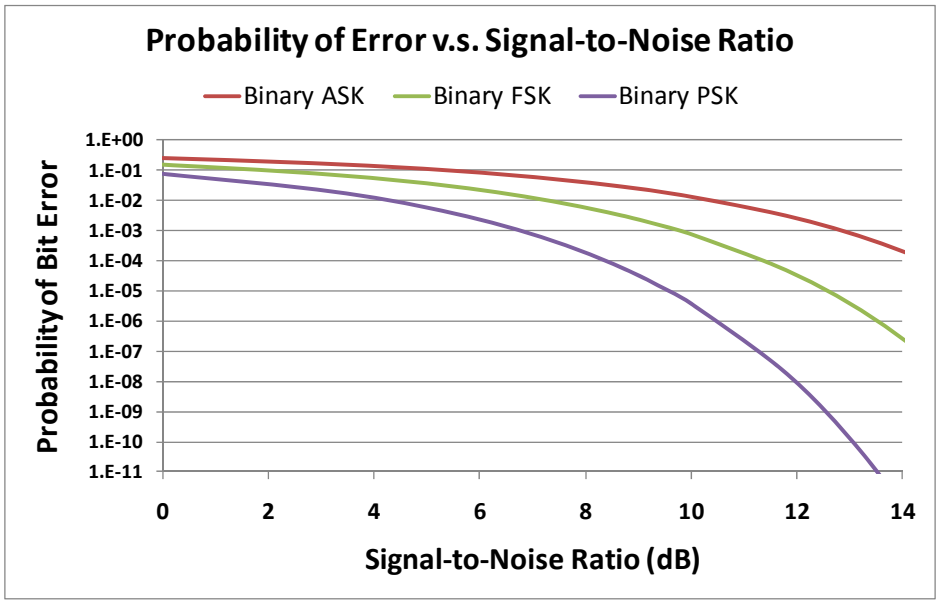


Figure 2-5: Probability of error versus signal-to-noise ratio for binary ASK, FSK and PSK modulations

From Table 2-1 and Figure 2-5, it is shown that the BPSK modulation has the advantage of better BER performance with the same received SNR than binary ASK and FSK. In addition, the BPSK modulation scheme is more efficient in terms of the occupied bandwidth and the transmitted power compared to binary FSK and ASK. In general, the BPSK-modulated passband signal occupies twice the baseband bandwidth. To further improve the bandwidth efficiency, a raised-cosine pulse-shaped filter could be implemented without sacrificing the BER performance. Table 2-2 provides a summary table of the current popular wireless technologies and it shows the prevalent applications of PSK and its variants [17] [18]. The rest of this section focuses on the practical implementation issues of the single- and multi-carrier demodulation techniques.

Table 2-2: Comparison summary of current wireless technologies [17] [18]

Technology and Standards	802.11 WLAN	Bluetooth WPAN	WiMAX	ZigBee WPAN	UMTS-3G
Frequency Band	2.4/5.8 GHz	2.4 GHz	2.5/3.65 GHz but not limited	868/915 MHz 2.4 GHz	1.7/2.1 GHz (America) 1.9/2.1 GHz (Worldwide)
Maximum Data Speed	248 Mbps w/ MIMO; 54 Mbps w/o MIMO	3 Mbps	134 Mbps (downlink)	250 Kbps	21 Mbps (downlink)
Modulation Techniques	BPSK/ QPSK/ QAM with OFDM	FSK/ QPSK/ 8-PSK	QPSK/16-QAM with OFDM	BPSK/ Offset QPSK	QPSK with W-CDMA

2.4.1 Single-Carrier Demodulator

In a typical single-carrier digital communication system, the DSP of the receiver contains several essential functional blocks shown in Figure 2-6. The timing and frequency synchronization corrects the minor phase offset and frequency drift in the sampled digital signal. The equalizer is used to mitigate the multi-path effect in the wireless channel. The amount of delay that can be tolerated by the demodulator system depends on the number of taps implemented in the equalizer. The QAM de-mapping function converts the transmitted symbol back into corresponding digital bits. Interleaving of the original digital bit stream allows the Viterbi's forward error correction (FEC) decoder to operate effectively against burst errors when the consecutive erroneous bits are spread out among all receiving bits. Hence a large extent of error correction can be attempted by the FEC decoder without triggering any data re-transmission. This architecture and its variants are commonly used in narrowband transmission such as the digital TV broadcast and cable modem terminal system (CMTS) as well as many proprietary communication systems such as point-to-point high-capacity microwave linking and satellite communication. By applying high-level modulation such as 256-QAM or 1024-QAM and heavy FEC coding (1/2), such demodulator design has a robust performance even under some harsh RF channel characteristics. However, this demodulator architecture suffers from the aforementioned power-budget issues (from power-hungry ADCs and DSPs) discussed in Section 1.2 as the transmission speed scales into the gigabit range.

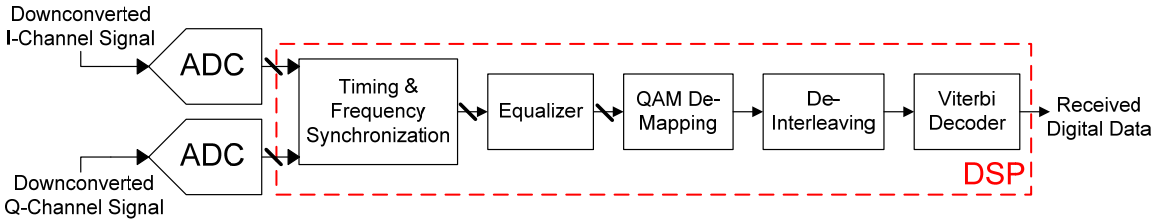


Figure 2-6: Block diagram of a generic single-carrier digital demodulator system

2.4.2 Multi-Carrier Demodulator

An alternative to the single-carrier system is the popular multi-carrier OFDM receiver architecture (shown in Figure 2-7), which has been currently adopted by several international standards: IEEE 802.11a/g, terrestrial digital video broadcasting (DVB-T) and digital audio broadcasting (DAB) [19]. The original serial high-speed data is first divided by the serial-to-parallel converter (S2P) into multiple (approximately 2^N) lower data-rate parallel channels. With the inverse Fast Fourier-transform (IFFT) at the transmitter, these time-domain data channels are first modulated (usually BPSK, QPSK, 16-QAM) then converted into frequency-domain channels. Afterwards, they are transmitted simultaneously using 2^N orthogonal frequency carriers. These carefully chosen frequency carriers are tightly packed on the spectrum and the orthogonal attribute ensures zero interference to their adjacent carriers without any guard band in between. At the receiver end, the DSP hardware of the advanced Fast-Fourier transform (FFT) reverses the time-domain to frequency-domain transformation and retrieves the original data stream. In an OFDM system, the multipath effect is reduced by using multiple lower-data rate channels, which have relatively longer delay spread. Hence it can tolerate the inter-symbol interference (ISI) caused by the multipath. In addition, a cyclic prefix is

implemented and it acts as a guard time before each OFDM symbol [19]. The benefits of these additional OFDM processing steps allow the communication system to work in a non-line-of-sight (NLOS) wireless environment as well as a clustered space without the needs of an equalizer, which is the main attraction of this modulation technique.

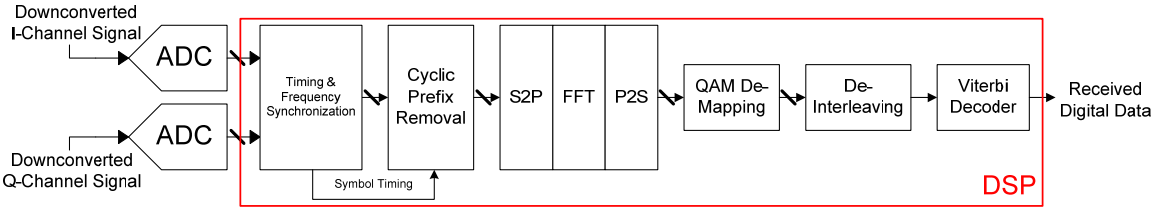


Figure 2-7: Digital block diagram of a typical multi-carrier OFDM demodulator system

One of the proposed UWB standards, MBOA has demonstrated a wireless throughput of 480 Mbps using 128 QPSK-modulated sub-carriers 4 MHz [2] [3]. Such demodulator requires two 1.1 GHz ADC's and FFT of 128 in the DSP. However, the same architecture cannot be easily scaled into the multi-gigabit range without the penalty of higher power consumption. With higher throughput, ADC's sampling speed is doubled or tripled and the clock rates of the DSP would also need to be adjusted accordingly.

2.5 CMOS IC Technology

III-V semiconductors have been the enabling technology that addresses the needs of microwave and millimeter-wave applications. However, as the aggressive CMOS process scaling continues with the ever-increasing digital microprocessor requirements, the advanced Si-based technologies now have comparable f_T and f_{MAX} as those high-performance InP, pHEMT and GaAs compound processes [20] (shown in Figure 2-8).

Unity-current-gain frequency, f_T, and maximum oscillation frequency, f_{MAX} of the active device are good performance indicators of the RF capability that the fabricated IC can operate at. Although the CMOS technology has the drawbacks of low transconductance (g_m), high flicker noise and low breakdown voltage, the low-cost advantage through high integration and huge backend digital processing capability allows the deep sub-micron CMOS to be the enabling platform for the rapidly-growing market of low-power portable wireless applications. As shown in the recent publications [21] [22] [23], separate RF functional blocks and integrated millimeter-wave front-ends (LNA, mixer, oscillator, frequency synthesizer even power amplifier) have been implemented and demonstrated in 90 nm and 65 nm CMOS. The multi-gigabit CMOS demodulator might not need to operate at such high frequencies but high f_T of the cutting-edge CMOS technology enables higher 3 dB cut-off frequencies (smaller Cgs due to shorter gate length) for the baseband amplifier and VGA without additional complicated bandwidth-enhancement techniques which requires more power and chip space [24]. Due to the fact that the standard digital CMOS process is optimized and characterized primarily for speed and power trade-off, analog and mixed CMOS IC design requires multi-dimensional considerations using the same process. Trade-offs between performance parameters of noise, linearity, gain, supply voltage, voltage swings, speed, input/output impedance and power dissipations need to be evaluated thoroughly and special attention is needed when the final optimal design is reached [25]. All proposed low-power multi-gigabit demodulators in this dissertation are designed and fabricated in 90nm standard CMOS process.

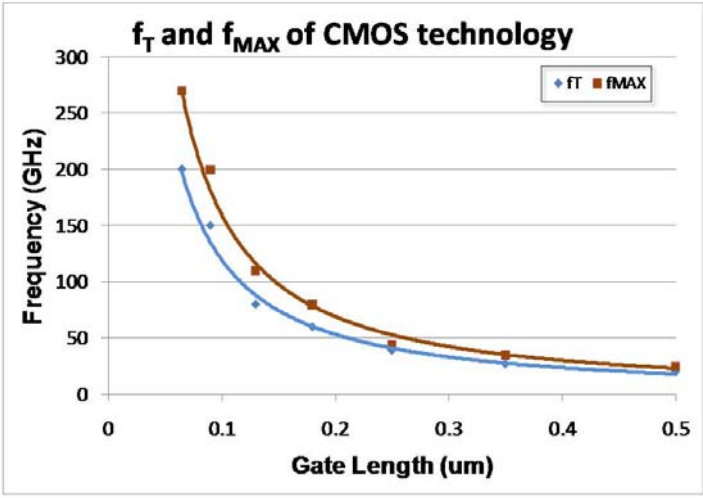


Figure 2-8: Typical f_T and f_{MAX} of CMOS devices at different technology nodes

2.6 Link Budget Analysis

In order to obtain an insight into the capability of a multi-gigabit system, the overall link budget is analyzed from the system-level parameters such as antenna gain, noise figure, transmitted power, minimum sensitivity, occupied RF bandwidth and coverage distance. According to the Friis free space propagation model with line-of-sight path [26], the received signal strength, p_R, can be expressed in the following linear and logarithmic forms

$$p_R = \frac{p_T g_T g_R \lambda^2}{(4\pi)^2 d^2 l} \tag{6}$$

$$P_R = P_T + G_T + G_R - 20\log_{10}(\frac{4\pi df}{c}) - L \tag{7}$$

where, p_T and P_T are the transmitted signal power in linear and logarithmic forms

g_T/g_R and G_T/G_R is the transmitter and receiver antenna gain in linear and logarithmic forms

λ and f is the wavelength (m) and frequency (Hz) of RF carrier

d is the distance (m) between the transmitter and the receiver

$[\lambda/(4\pi d)]^2 = [c/(4\pi df)]^2$ is the free space loss

l and L are the additional implementation loss in linear and logarithmic forms

It indicates that the transmitted power has to be increased by four times to double the coverage distance. However, emission limits on the transmitted output power are imposed by the local regulatory bodies in the form of maximum allowable effective isotropic radiation power (EIRP). EIRP is defined as

$$EIRP = p_T g_T \tag{8}$$

For example, the emission power requirement for license-free 60 GHz is shown in Table 2-3. In general, an isotropic antenna radiates equally in all directions but it is more desirable for a multi-gigabit wireless system to concentrate its antenna radiation coverage to certain directions. With an optimized antenna design, the antenna gain increases with a smaller beamwidth. Hence, high EIRP and large coverage distance can be achieved by narrow-beamwidth antennae without interfering other nearby data transmissions using similar frequency carriers. Traditionally, high-gain point-to-point antennae are large in size. However, with carrier frequency in the range of GHz, a small form-factor integrated printed antenna is possible with LCP or LTCC materials and this is especially important for portable applications. In addition, adaptive phase-array with beam-steering algorithm can be applied to further increase the coverage and robustness of the system.

Table 2-3: Emission power requirements [27]

Region	Output Power	Other Restrictions
Australia, Canada and U.S.A	10 mW into antenna 500 mW peak	150 W (51.8 dBm) peak EIRP Min. BW=100 MHz
Japan	10 mW into antenna	47 dBi max. antenna gain
Europe	57 dBm EIRP	Min. BW=500 MHz

The minimum sensitivity of a wireless receiver is determined by the noise figure of the RF/analog front-end, the minimum signal-to-noise ratio requirement for intended demodulation and the occupied RF bandwidth. It is given by

$$S_{MIN} = 10\log_{10}(KT) + NF + 10\log_{10} B + SNR_{MIN} \quad (9)$$

where, K is the Boltzmann constant= 1.380×10^{-23} Joule/K

T is the absolute temperature measured in Kelvin

NF is the noise figure of the RF-analog front-end before the demodulation begins

B is the bandwidth over which the transmitted RF signal occupies

SNR_{MIN} is the minimum signal-to-noise ratio required for the chosen modulation

The first three terms define the noise floor of the receiver, which is the integrated noise power that the demodulator needs to contend with for a proper recovery of the transmitted bitstream.

Table 2-4 shows the generic link budget analysis of the 1 Gbps wireless system operating in the upper UWB band (which is accepted in more regions worldwide) and 60 GHz with some reasonable assumptions. Although the carrier frequency of the UWB

system is lower in comparison, i.e. smaller free-space loss, the maximum coverage distance is slightly poorer with a limited EIRP of -41.3 dBm/MHz. However, the additional loss due to the oxygen absorption needs to be accounted for in the 60 GHz band. In fact, it could result in a few dB of degradation in the link budget calculation, which significantly reduces the coverage of the multi-gigabit system at such high frequencies. Furthermore, the system implementation loss as high as 5~10 dB should also be considered in order to give a more realistic prediction of the actual performance. Ultimately, the link budget analysis provides a performance abstract of the wireless multi-gigabit system that brings various circuit- and system-level issues together.

Table 2-4: Link budget analysis for the multi-gigabit systems operating in the upper UWB and millimeter-wave 60 GHz bands

Technology	**UWB**	**Millimeter-wave 60 GHz**
Carrier Frequency	8 GHz	60 GHz
Data Speed & Modulation	1 Gbps, BPSK	1 Gbps, BPSK
RF Bandwidth	2 GHz	2 GHz
NF of the Receiver	7 dB	10 dB
Noise Floor of the Receiver	-73 dBm	-70 dBm
Signal-to-Noise Ratio	10.5 dB @ 1×10^{-6}	10.5 dB @ 1×10^{-6}
Minimum Sensitivity	-62.5 dBm	-59.5 dBm
Transmitted Power	-8.3 dBm	10 dBm
Total Antenna Gain (G_T+G_R)	6 dBi	10 dBi
Theoretical Maximum Distance	3 m	3.7 m
Free-Space Loss	60 dB	79.4 dB
Line-of-Sight Received Power	-62.2 dBm	-59.4 dBm
Link Margin	0.3 dB	0.1 dB

2.7 Summary

In this chapter, UWB and millimeter-wave technologies are introduced as the potential operating frequencies for low-power multi-gigabit system. Their individual channel characteristics are discussed in details as the UWB signal is restricted by the regulated EIRP and the millimeter-wave frequencies are limited by the additional loss due to water or/and oxygen molecules. Heterodyne and direct-conversion receiver architectures are presented as the realization of the proposed multi-gigabit 60 GHz and UWB system respectively. Different (amplitude, frequency and phase) digital modulation schemes are described and compared in terms of their power and bandwidth efficiencies. In addition, traditional digital single- and multi-carrier demodulation techniques are explained and analyzed. It is also shown that these approaches are not suitable for scaling up to the multi-gigabit level. It further emphasizes the importance of low-power analog demodulator alternative in the ultra-portable applications. Finally, a link budget analysis using realistic system parameters is provided for the potential multi-gigabit UWB and 60 GHz system to demonstrate the trade-off between coverage distance and speed.

Chapter III

Analog Quadrature Front-End

3.1 Introduction

The I-Q or quadrature receiver topology is one of the most commonly-used architectures in either super-heterodyne or direct-conversion receiver. This is due to the popularity of QPSK and QAM modulation schemes employed in various communication systems from low data-rate to high-speed applications. The benefit of two orthogonal carriers provides opportunities of innovative analog and/or digital signal processing techniques for high-speed demodulation techniques. The quadrature LO generation can be easily achieved in IC technology in contrast to the traditional approach of discrete components. Hence, all essential building blocks of the quadrature receiver architecture (as shown in Figure 3-1) are implemented in CMOS. The main function of the quadrature receiver is frequency down-conversion that brings the modulated passband signal to the baseband frequency regardless of the LO coherency. These building blocks, i.e. mixers, quadrature VCO and baseband amplifiers (as well as VGA) were first designed using 1.8V power supply to evaluate their feasibilities. However, low-power circuit design based on 1V power supply is needed to reduce the overall DC power consumption without significant performance degradation of the broadband requirement. The target

specification of the wideband quadrature receiver is a baseband bandwidth of more than 1.5GHz under 100mW of DC power consumption.

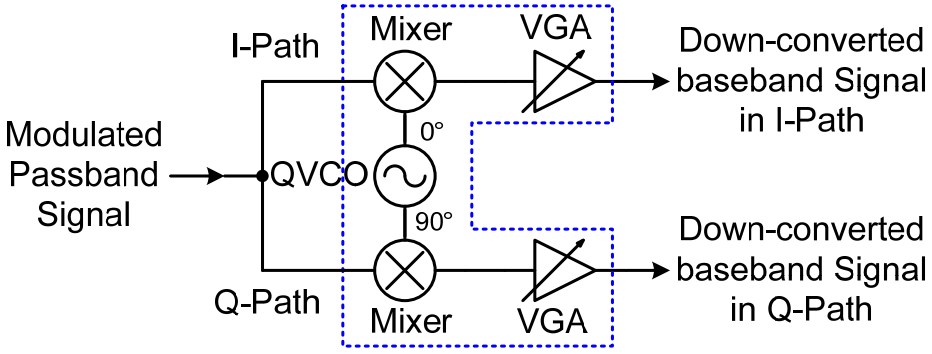


Figure 3-1: Quadrature receiver architecture

CMOS mixer design is detailed in Section 3.2 and several different baseband amplifier architectures are discussed in Section 3.3. QVCO circuits and its performance are presented in Section 3.4. Measurement results of the analog quadrature front-end in 1.8V and 1V supply voltage are compared in Section 3.5.

3.2 Mixer

Mixer performs the critical function of frequency translation that brings the incoming modulated IF or RF carrier signal(s) to the baseband for demodulation purposes. Several important parameters of a mixer design are conversion gain and bandwidth, linearity (measured in input P_{1dB}) and DC power consumption.

3.2.1 Gilbert-Cell Architecture

The down-conversion mixer for 1.8 V is a widely used double-balanced Gilbert-cell architecture shown in Figure 3-2(a) [28]. Switching transistors, namely M3-M6 are driven by the LO± and they vary the drain currents of M1 and M2, whose gates are connected to the RF± inputs. Capacitors C1 and C2 provide the low-pass filtering of any high-frequency mixing products at the differential outputs. However, this same circuit topology cannot be used in the 1 V low-voltage supply due to the linearity-to-conversion-gain trade-off. Since the voltage drop across the load resistors, R1 and R2, is limited by the supply headroom, a double-balanced Gilbert-cell mixer suffers a low conversion gain using a 1 V supply. For example, the quiescent point of the differential IF± outputs is ideally chosen as the mid-point between $v_{DS1}+v_{DS3}+v_{DS7}$ and VDD to provide the best linearity without forcing any transistors out of the saturation region. When VDD is changed from 1.8 V to 1 V, the $v_{DS1}+v_{DS3}+v_{DS7}$ stays as the lower limit hence the maximum output swing of the mixer is immediately reduced by more than 50%. With the removal of the current sink transistor shown in Figure 3-2(b), a marginal improvement in the conversion gain is possible. However, the linearity of such mixer is degraded at the same time. This can be shown in Figure 3-2(c), in which the input is a single-tone signal at RF±, output A and B represents the differential voltage at drains of M1-M2 in Figure 3-2(a) and Figure 3-2(b) respectively. At a low input power level, both output waveforms show similar behaviors. As the input power level increases, the mixer in Figure 3-2(b) begins to experience clipping during the negative cycle due to a limited overdrive voltage of M1 and M2. This forces the transistors M1 and M2 out of saturation and into linear or

sub-threshold regions or even off-state. Hence a different mixer circuit topology is required for 1 V supply to have a comparable linearity performance.

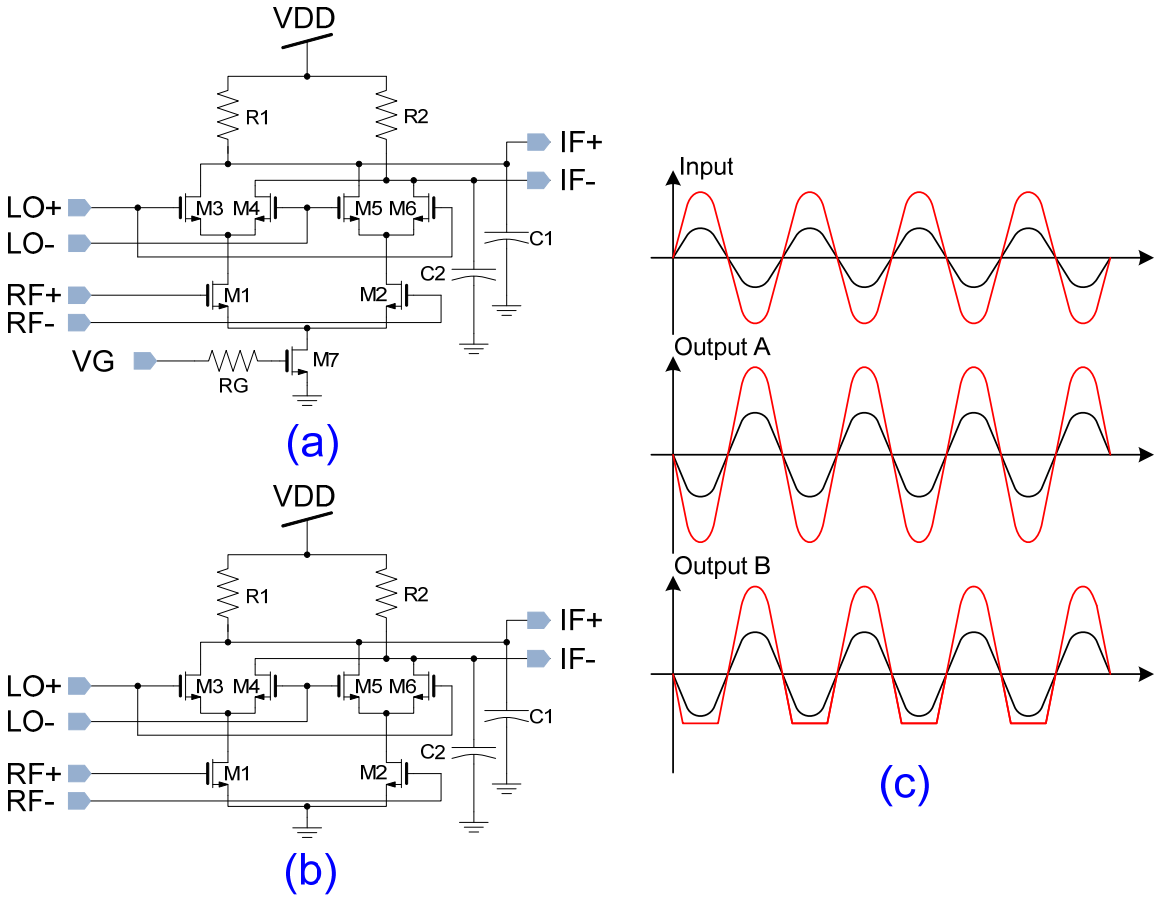


Figure 3-2: (a) Double-balanced Gilbert-cell mixer design in 1.8 V power supply; (b) removal of the current-sink in (a) for 1 V power supply operation; (c) waveforms of the two mixers in (a) and (b)

3.2.2 Low-Voltage Mixer

Figure 3-3 depicts the schematic of the double-balanced mixer circuit for 1 V power supply [29]. This mixer exhibits greater linearity due to the passive mixing of transistors, M1-M4. The linear baseband amplifier compensates its loss. The degenerative

amplifier also acts as a buffer for the mixing core. Table 3-1: shows the performance comparison between the two mixers, namely Gilbert-cell mixer in 1.8 V and passive mixer in 1 V. Figure 3-4(a) shows the simulated conversion gain and the down-converted bandwidth of both mixers and Figure 3-4(b) and Figure 3-4(c) show the simulated P_{1dB} of the two mixers. As Table 3-1: shows, the 1 V passive mixer has a comparable performance with respect to its 1.8 V counterpart but it draws less current. It should be noted that the conversion gain of the 1 V passive mixer can be easily increased by reducing the value of the resistors, R7 and R8. Currently, the gain was set for the overall system design.

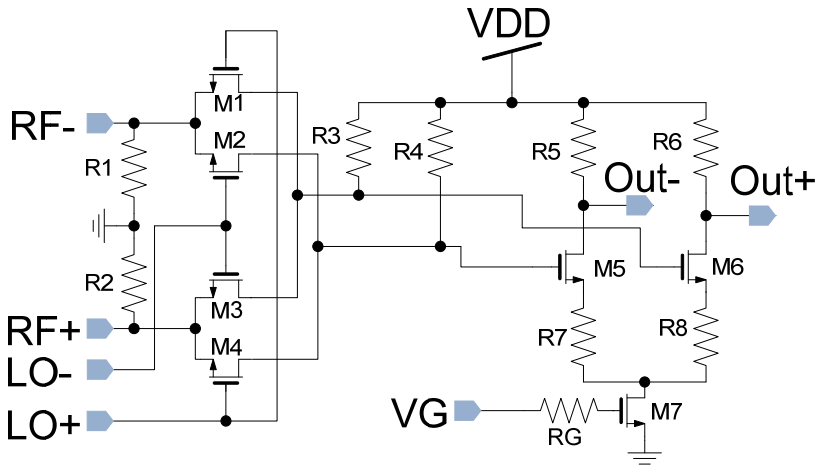


Figure 3-3: Double-balanced passive mixer for 1 V power supply operation

Table 3-1: Performance comparison of the two mixers

	Gilbert-cell Mixer in 1.8 V	**Passive Mixer in 1 V**
Conversion Gain	6 dB	3 dB
Power Consumption	7.6 mW (1.8 V)	4 mW (1.0 V)
Single Sideband Bandwidth	3 GHz	4 GHz
Input P_{1dB}	500 mVpp	320 mVpp

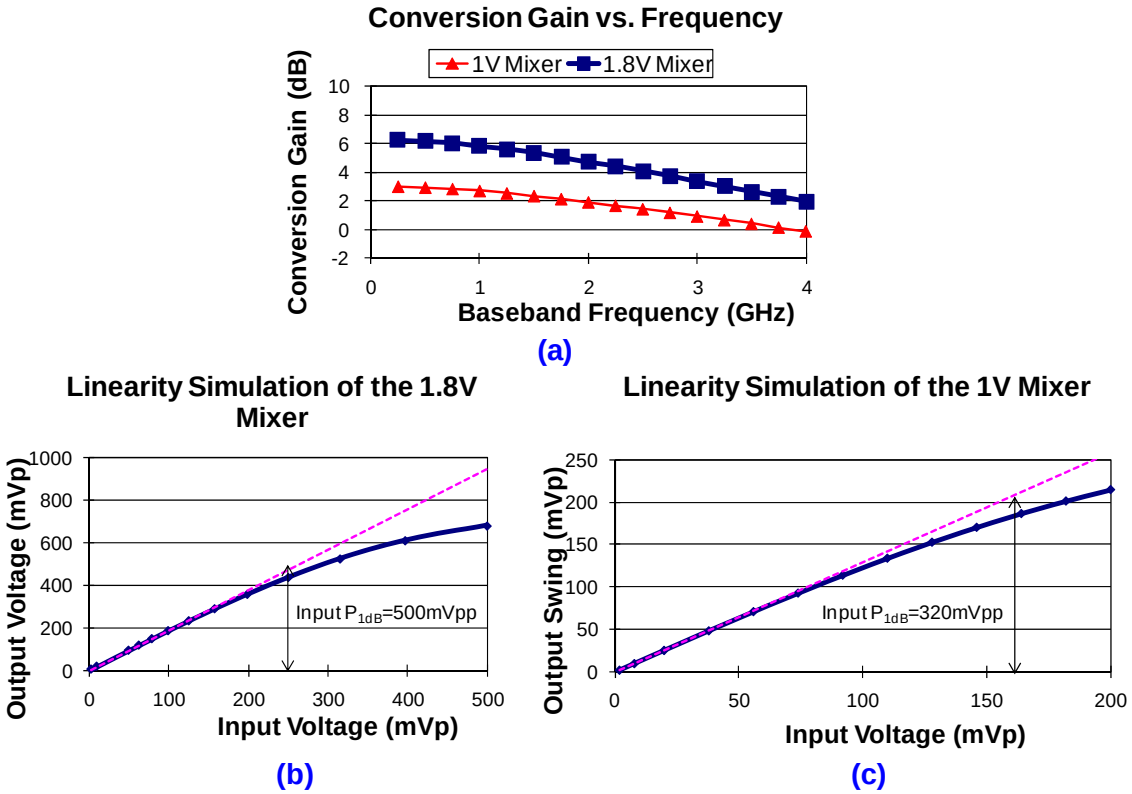


Figure 3-4: (a) Simulated conversion gain and down-converted bandwidth; (b) linearity simulation of the 1.8 V mixer; (c) linearity simulation of the 1 V mixer

3.3 Baseband Amplifiers

The main function of the baseband amplifier(s) inside the quadrature receiver is to augment the down-converted baseband signal, i.e. at the mixer output, with high gain while maintaining good linearity and decent bandwidth.

3.3.1 Cherry-Hooper Amplifier Architecture

The variable-gain amplifier (VGA) (shown in Figure 3-5) is based on the Cherry-Hooper architecture with source-follower feedback [30]. Resistors R5 and R6 increase

the gain of the amplifier without significantly impacting the bandwidth. The frequency response of the source-follower feedback path (transistors M3 and M4) exhibits a wider bandwidth than that of the common-source amplifier formed by transistors M5 and M6 [31]. As a result, the pole caused by C_{gs3} and C_{gs4} is much higher than the overall amplifier bandwidth and therefore can be ignored. The half-circuit small-signal low-frequency gain is given by

$$Out+/In- = \frac{g_{m1}(R_3 + R_5)(1/g_{m3} + R_1)}{2(1/g_{m5} + R_3)} \tag{10}$$

Transistors M7, M8 and M9 are used to provide a variable degeneration in the differential signal path and their widths determine the amount of attenuation. Gates of transistors (GC0-GC2) are digitally controlled by turning them ON or OFF individually but a continuous voltage control is also possible. Figure 3-6(a) shows the simulated P_{1dB} of the Cherry-Hooper amplifiers whereas Figure 3-6(b) depicts its simulated frequency responses. Table 3-2 shows the performance summary of the Cherry-Hooper amplifier in 1.8 V.

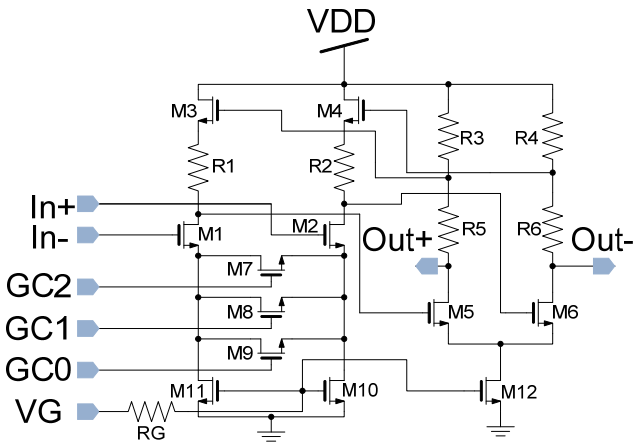


Figure 3-5: Variable-gain amplifier based on the Cherry-Hooper architecture with source-follower feedback in 1.8 V operation

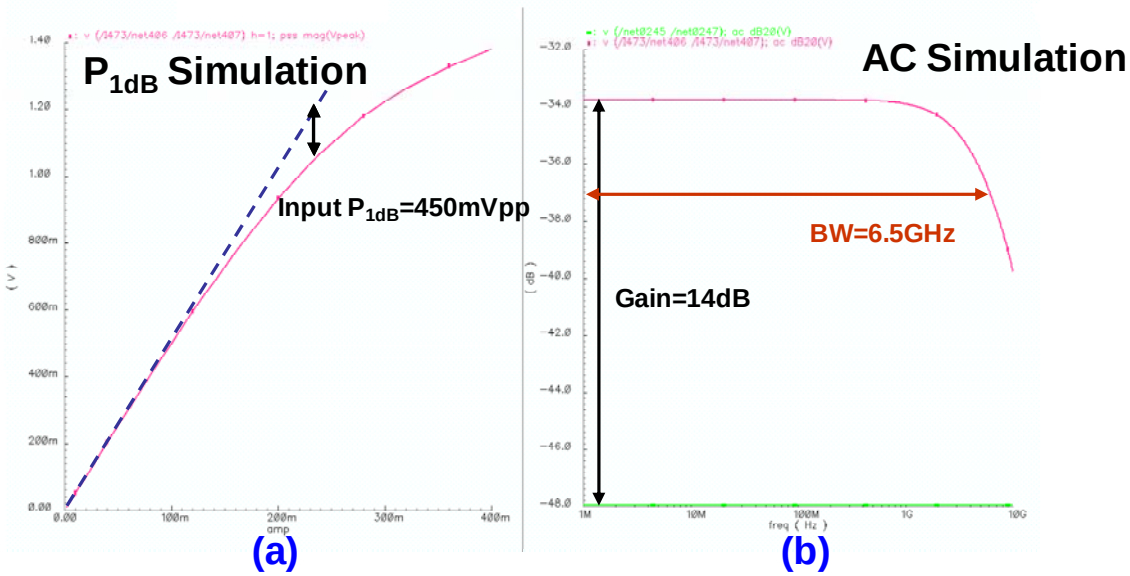


Figure 3-6: Simulated performance of the Cherry-Hooper variable gain amplifiers in 1.8 V supply: (a) linearity simulation; (b) frequency response

Table 3-2: Simulation performance of the Cherry-Hooper variable gain amplifier

Maximum Gain	14.2 dB
Power Consumption	12 mW (1.8 V)
Bandwidth	6.5 GHz
Input P_{1dB}	450 mVpp @ max. gain
Gain Variation	5 dB

3.3.2 Automatic Gain Control

The aforementioned Cherry-Hooper architecture cannot be translated into low-supply voltage design due to the reduced headroom by the source-follower. For the same reason, the gain of a single-stage amplifier is limited while operating at 1 V. Therefore, the baseband amplification must be realized using multiple cascaded gain stages. Figure 3-7 shows the AGC amplifier used in the quadrature analog down-converter. Each of the quadrature

signal path consists of three cascaded differential amplifiers (DA1) with DC offset compensation feedback inserted between the outputs of the first and third gain stages. The DC offset compensation is a low-frequency feedback loop intended to maintain the DC operating point of each gain stage relatively constant amid the mismatch in the differential signal path. This control mechanism is critical for mitigating signal distortion or potential oscillation especially when dealing with high-gain as a result of multiple cascaded gain stages. There is another feedback loop that keeps the output power of the AGC to a required level. The power detector senses the output power of the baseband and in turn produces a corresponding DC voltage, which is then compared with an external gain control voltage by the operational amplifier (OPAMP). The OPAMP output adjusts either amplification or attenuation of all gain stages accordingly.

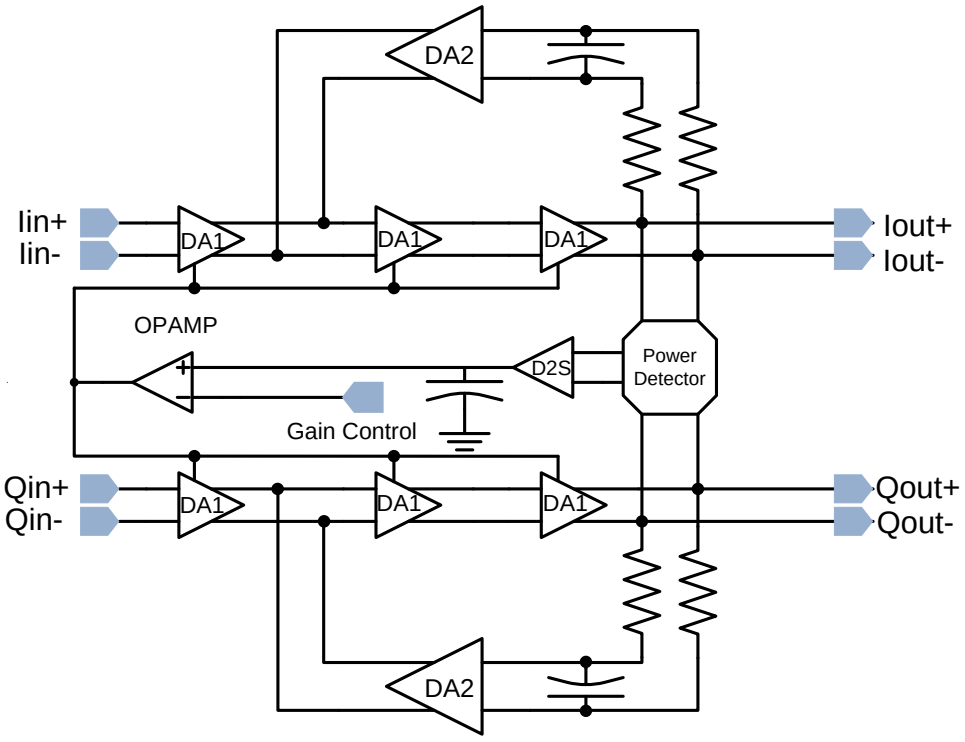


Figure 3-7: Functional blocks of the automatic-gain control amplifiers in 1 V

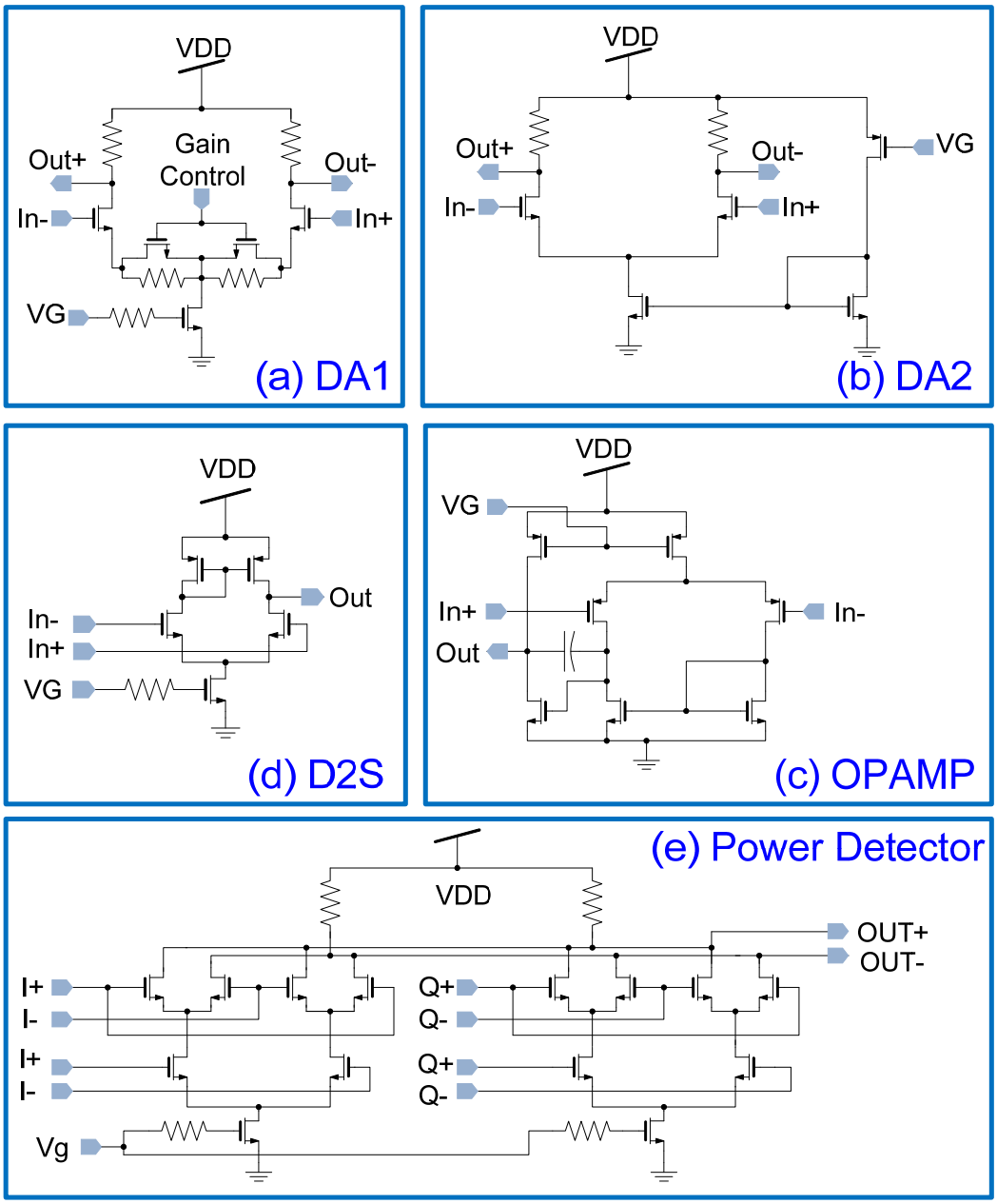


Figure 3-8: Circuits of the individual functional blocks in AGC: (a) differential amplifier gain stage (DA1); (b) differential amplifier (DA2); (c) operational amplifier (OPAMP); (d) differential-to-single-ended converter (D2S); (e) power detector

The individual circuits of the AGC are shown in Figure 3-8. Each gain stage, DA1, is a wideband differential amplifier with variable resistor degeneration by the

control voltage. On the contrary, DA2 (shown in Figure 3-8(b)) has a relative lower cutoff frequency (in MHz range). It is used for the DC offset compensation with the two resistors and a capacitor (forming a low-pass filter response to the differential signal) at the quadrature outputs of the AGC. The automatic gain control loop comprises of three major components, namely, OPAMP, the differential-to-single-ended converter (D2S) and the power detector. The power detector circuit (shown in Figure 3-8(e)) consists of two double-balanced Gilbert-cell mixers with a common differential load. Each half circuit performs the squaring function by connecting the gates of the upper-stack and lower-stack transistors to the same input signal. The output of the power detector produces a summation of squared quadrature signals (i.e. I^2+Q^2). At the output of the D2S, an additional capacitor is used to remove any high-frequency component from the detecting power-level voltage and this helps avoid the jittering response to a changing gain-control voltage.

Figure 3-9(a) and (b) illustrate the simulated P_{1dB} and the frequency response of the AGC operating in 1 V supply. Figure 3-10(a) and Figure 3-10(b) show the simulated time-domain output waveforms and the corresponding control voltage (connected to the "Gain Control" port of DA1 in Figure 3-8(a)) of the AGC respectively at various gain-control settings. Table 3-3 summarizes the overall simulated performance of the AGC. In comparison to the baseband amplifiers operating in 1.8 V supply, the AGC provides a higher gain with more than 2 GHz of bandwidth at similar DC power consumption.

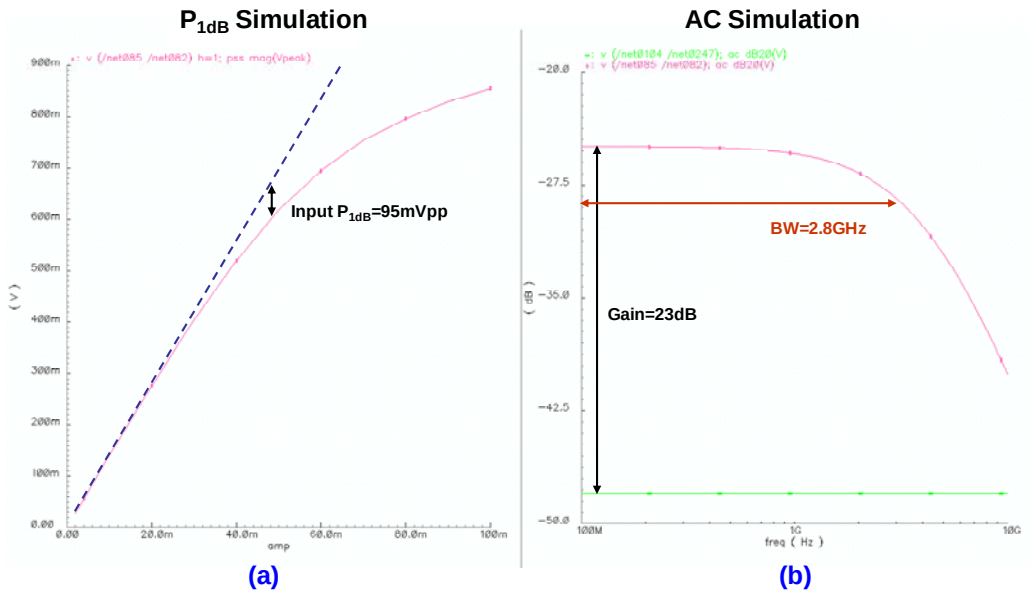


Figure 3-9: (a) Linearity simulation; (b) simulated frequency response of the AGC

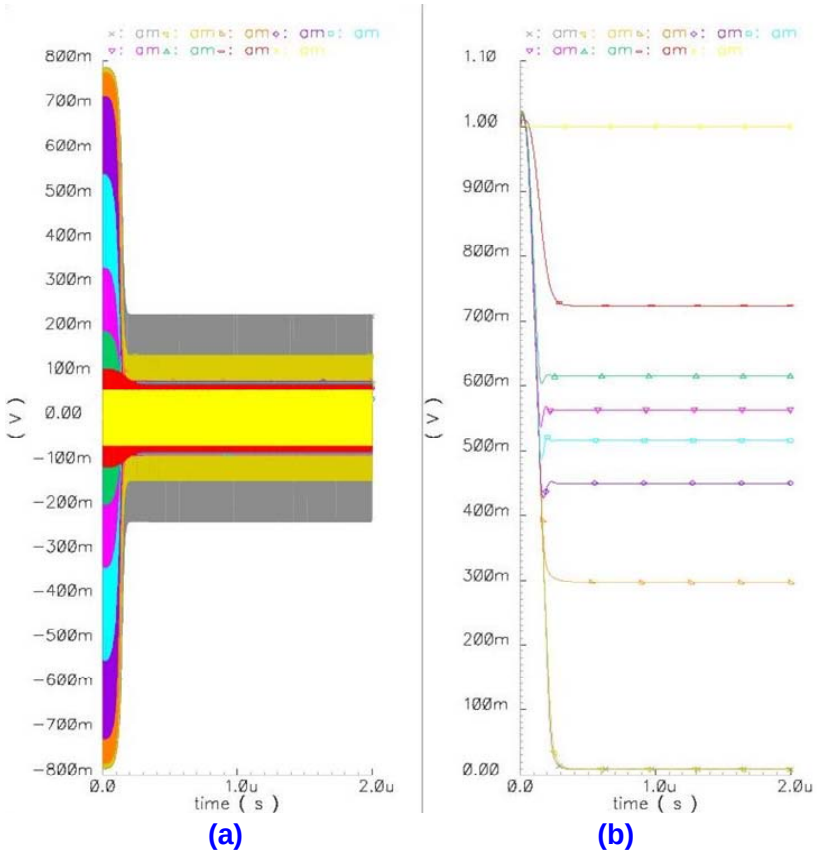


Figure 3-10: (a) Time-domain differential output signal waveform of the AGC; (b) the corresponding control voltage behavior of the AGC at various gain-control settings

Table 3-3: Simulation performance of the AGC in 1 V

Maximum Gain	23 dB
Power Consumption	25 mW Overall (1.0 V)
Bandwidth	2.8 GHz
Input P_{1dB}	95 mVpp@ maximum gain
Gain Variation	27 dB

3.3.3 Bandwidth Extension Technique

One of the main disadvantages of cascading multiple gain-stages is the reduction of the overall signal bandwidth. Several broadband techniques have been invented for high-speed IC applications. Among them, inductive peaking is one of the popular methods to significantly increase the bandwidth of the gain stages. However, an on-chip inductor takes up large die-space and it makes surrounding routing difficult with increasing parasitic effect. With the limited chip real-estate in mind, inductive peaking can also be achieved by using active devices, called active inductor, however it is impossible to utilize such circuit at supply voltage below 1.5 V [24]. Therefore, a different alternative broadband solution is required for similar bandwidth improvement at low supply voltage without sacrificing the space.

The resistive-capacitive (RC) degeneration in a differential pair (shown in Figure 3-11) has its transconductance (g_m) increasing at high frequencies. It offsets the gain roll-off due to the output pole of the simple amplifier's frequency response. The effective small-signal g_m (with RC degeneration) is given by

$$g_m = \frac{g_{m1}(R_3C_1s+1)}{R_3C_1s+1+g_{m1}R_3/2} \tag{11}$$

The zero, $1/(R_3C_1)$, of the transconductance can be strategically placed to cancel the pole at the output node hence the overall bandwidth is increased by a factor of $1+g_{m1}R_3/2$. However, the extended bandwidth comes at the cost of a proportional reduction in the overall small-signal gain. Another benefit of the RC-degeneration amplifier is a lower loading capacitor seen from the preceding stage because of the change in the input impedance. Hence the pole created by the previous gain stage can be relocated to higher frequency. The results are the improved overall signal path bandwidth for the two cascaded gain stage, i.e. itself and the preceding one. Figure 3-12 shows the comparison between the frequency responses of the standard differential-pair and the RC-degenerative gain stage. Both methodologies draw 4 mA from a 1 V source with the same output loading. However, the RC-degenerative amplifier has more than twice the bandwidth of the differential pair at the cost of 4 dB lower gain.

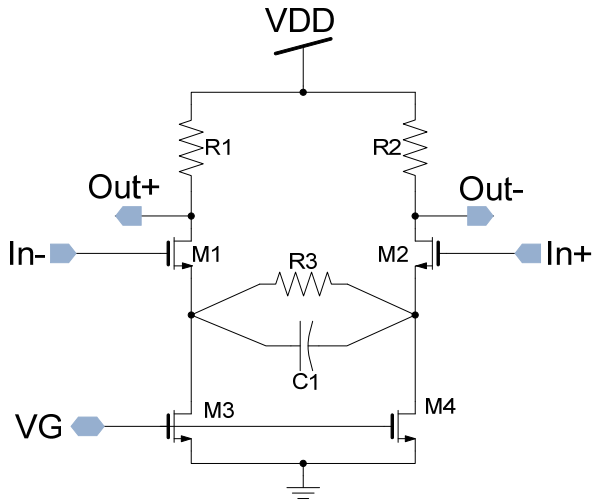


Figure 3-11: Broadband technique using RC degeneration in differential pair

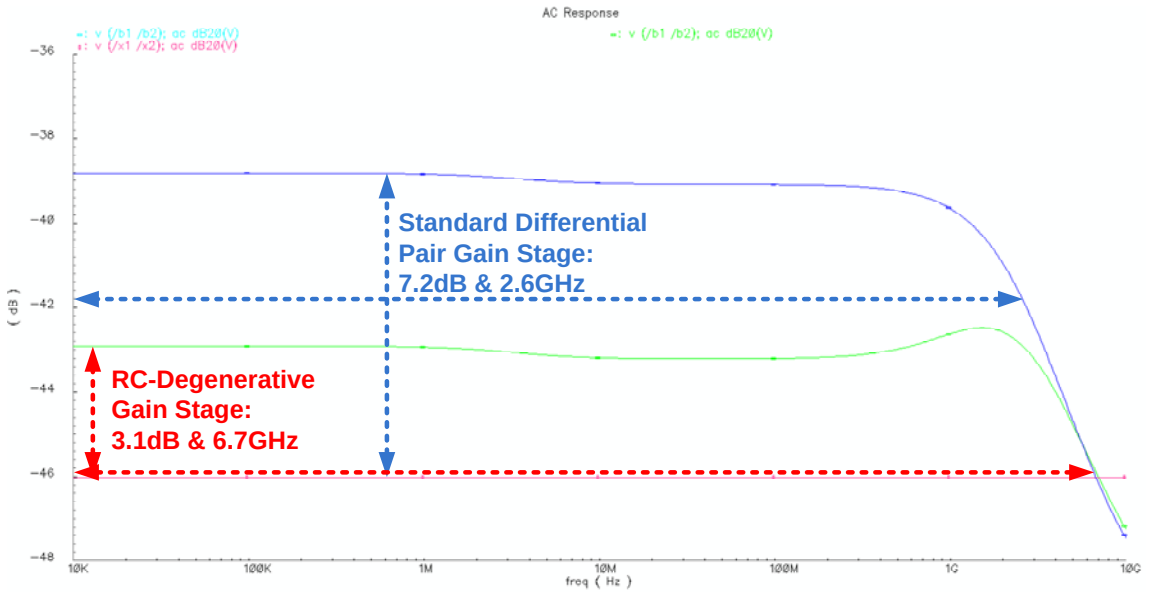


Figure 3-12: Frequency responses of the standard differential-pair gain stage and the RC-degenerative gain-stage

3.4 Quadrature Voltage Controlled Oscillator

Oscillators are a critical part of any wireless transceiver as it generates LO for the frequency down-conversion. The QVCO designs in 1.8 V and 1 V power supply are shown in Figure 3-13(a) and Figure 3-13(b) respectively. Core of two QVCOs is the same with a minor difference of the current sink, M13, in the 1.8 V version. The parallel cross-coupled NMOS and PMOS pair (transistors M1-M8), produces a negative resistance triggering the oscillation as well as the generation of quadrature LO signals [32]. The varactor pairs, V1-V2 and V3-V4, together with the inductors, L1 and L2, form the LC-tank resonator. Transistors, M9-M12, are used as the differential output buffer for the QVCO.

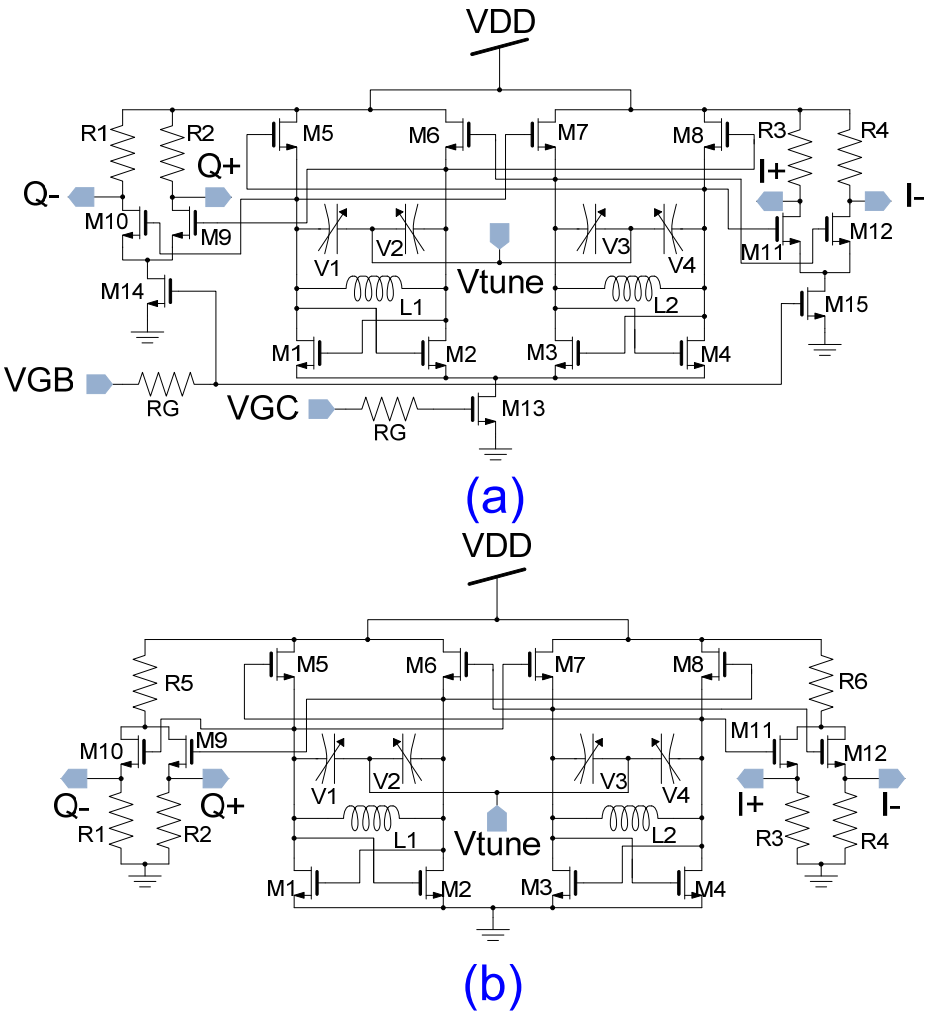


Figure 3-13: Circuit schematic of (a) quadrature VCO in 1.8 V; and (b) quadrature VCO in 1 V

Table 3-4 shows a performance comparison between the two QVCOs. As seen from the table, the two QVCOs have similar performance metrics. For demonstration and performance evaluation purposes, these QVCOs are designed to be used for upper UWB frequencies. In addition, the upper UWB frequency spectrum (7~10 GHz) are available throughout the world in comparison to the lower UWB band below 7 GHz, which allocated differently in various parts of the world. Figure 3-14 depicts the measured

tuning curves of the two QVCOs whereas Figure 3-15 shows the simulated phase noise numbers of the two QVCOs.

Table 3-4: Performance comparison of the two QVCOs

	QVCO in 1.8 V	**QVCO in 1 V**
Output Power	800 mVpp, differential	800 mVpp, differential
Power Consumption	22 mW (1.8V)	15 mW (1.0 V)
K_{VCO}	2 GHz/V	3 GHz/V
Phase Noise @ 1MHz offset	-95.6 dBc	-100.1 dBc

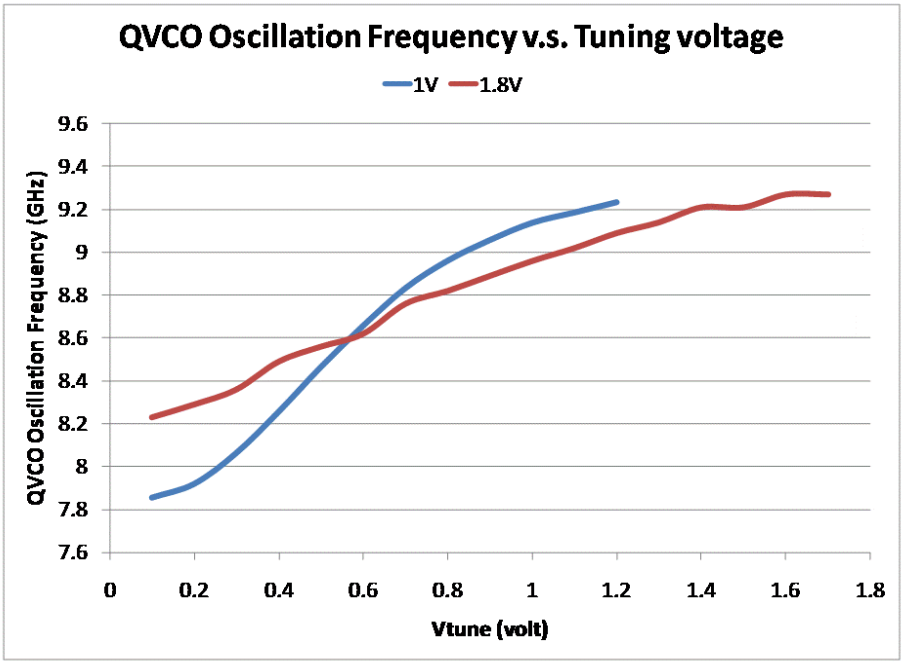


Figure 3-14: Measured tuning curves of the two QVCOs

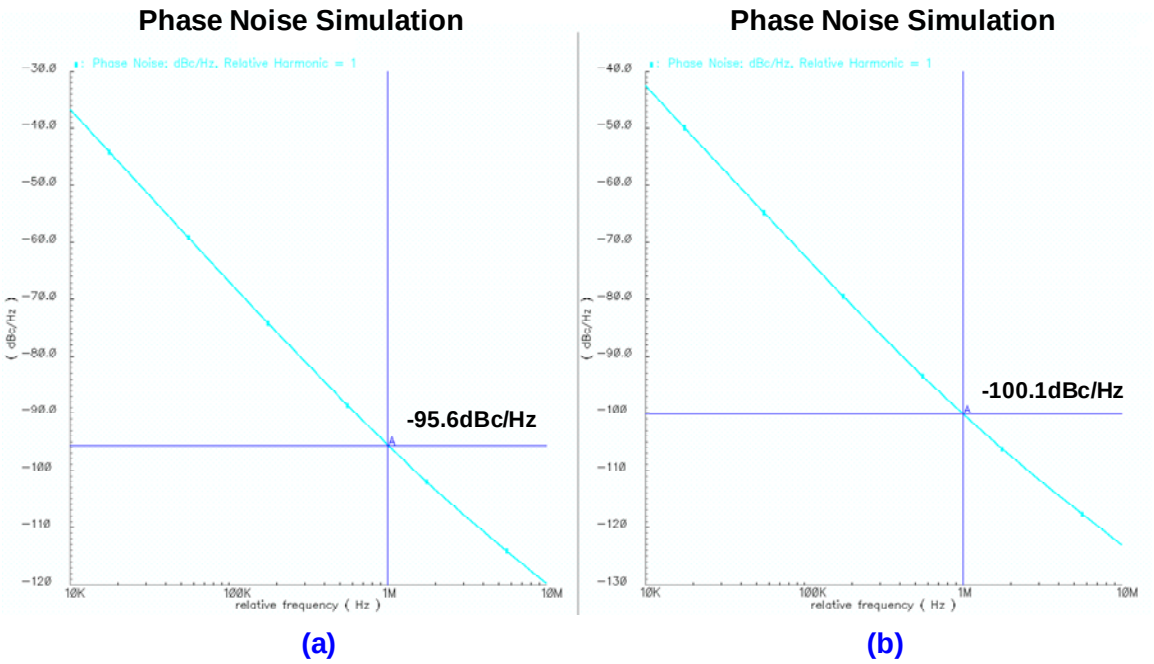


Figure 3-15: Phase noise simulation of (a) QVCO in 1.8 V supply; (b) QVCO in 1 V supply

3.5 Performance of the Analog Quadrature Front-End

Quadrature receivers operating at 1.8 V and 1 V supply voltages are fabricated in 90 nm CMOS and the photos of the IC chips are shown in Figure 3-16. The 1.8 V quadrature receiver consists of two mixers of Figure 3-2(a) with degenerative gain switching control, two baseband amplifiers of Figure 3-5 and one QVCO of Figure 3-13(a). The 1 V analog quadrature receiver consists of two mixers of Figure 3-3, one AGC of Figure 3-7 and one QVCO of Figure 3-13(b). The physical size of the 1.8 V version is 0.7 mm × 0.8 mm and 0.5 mm × 0.8 mm for the 1 V version.

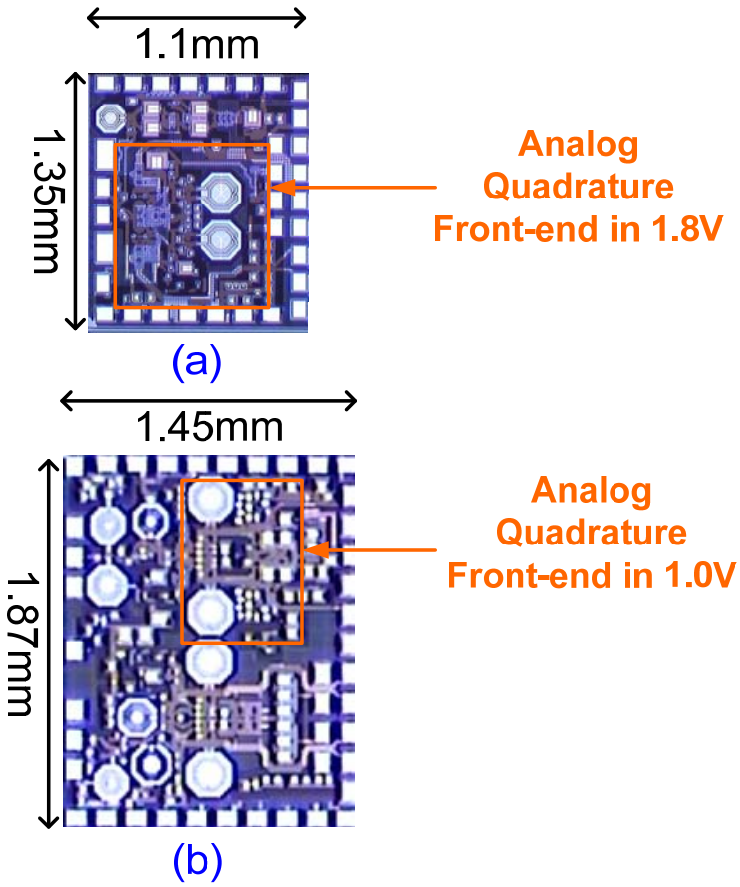


Figure 3-16: Photo of the analog quadrature front-ends: (a) 1.8 V version; (b) 1 V version

The measurement and simulation results of the two analog quadrature front-ends are shown in Table 3-5. As shown from the comparison, the 1 V analog down-converter achieves similar wideband performance at a lower DC power consumption. Both receiver front-ends have a baseband bandwidth over 1.5 GHz and a conversion gain around 20 dB. The dynamic range specification is important when the analog quadrature front-end is used with external ADCs.

Table 3-5: Measured and simulated analog quadrature front-end performance

	1.8 V Quadrature Receiver		**1 V Quadrature Receiver**	
	Measurement	Simulation	Measurement	Simulation
Conversion Gain	18 dB	20 dB	25 dB	25 dB
Power Consumption	58 mW (1.8 V)	61 mW (1.8 V)	46 mW (1 V)	48 mW (1 V)
Bandwidth	1.7 GHz	2.4 GHz	1.8 GHz	2.3 GHz
Input P_{1dB}	-9 dBm	-10 dBm	N/A	-17 dBm
Dynamic Range	11 dB, discrete	10 dB, discrete	23.3 dB, continuous	27 dB, continuous

3.6 Summary

A CMOS analog quadrature front-end has been designed and fabricated in 90 nm CMOS technology. It exhibits an IF-to-baseband conversion gain of 25 dB with 1.8 GHz of baseband bandwidth and a dynamic range of 23 dB while consuming only 46 mW from a 1 V supply voltage.

Chapter IV

Non-Coherent Demodulator

4.1 Introduction

The non-coherent demodulator is able to recover the original transmitted digital bitstream with no provision of carrier phase recovery, i.e. requires no synchronization between the transmitter's and receiver's LOs. Without the needs of carrier recovery, the demodulation can be achieved by using simple power detection method. However, for the same reason, the sensitivity of a non-coherent demodulator is worse than the coherent demodulator due to a SNR penalty resulting from distortion in the transmission medium such as multipath effect.

Section 4.2 describes the architecture and circuit implementation details of a non-coherent ASK demodulator that uses straightforward power-detector method. Another type of non-coherent ASK (and DBPSK with simple signal processing) demodulator is shown in Section 4.3 and it is compatible with the analog quadrature front-end mentioned in the Chapter 3. Measurement results of both demodulators are presented to compare the performance here.

4.2 Non-Coherent ASK Demodulator

ASK-modulated signals embed the original data stream in the envelope of its carrier. Hence it can be demodulated by a simple envelope or power detector. Despite many drawbacks of the ASK such as its susceptibility to noise and higher linearity requirement of the transmitter power amplifier, the simplicity of its demodulator makes it a primary candidate to demonstrate the feasibility of a new technology like gigabit wireless applications [33].

4.2.1 Architecture

The non-coherent multi-gigabit ASK demodulator is shown in Figure 4-1(a). This architecture is inspired by the frequency discriminator that was used for digital frequency modulation (FM) demodulation [34] [35]. The active bandpass filter (BPF) is used to eliminate the undesired RF signal blockers or other interference at similar frequencies in proximity. The squaring function acts as a power detector that distinguishes the existence of the ASK-modulated (Figure 4-1(a)) carrier (indicating a logic 1) from the null (indicating a logic 0) as shown in Figure 4-1(c). The following limiting amplifiers further boost the amplitude of the detected baseband signal (Figure 4-1(d)) so it is sufficient for the analog inverters to condition the demodulated baseband signal into 1's and 0's. The AC-coupling capacitor removes the DC component of the amplified signal, so a proper DC triggering voltage can be set at the input of the first analog inverter. Due to the size limitation of the on-chip capacitor, only one 15 pF capacitor is used here, therefore there is a high-pass effect to the demodulated AC-coupled baseband signal. However, such

effect would be minimal at higher transmission speed (≥400 Mbps) as most signal content of a digital bitstream is concentrated at the lower frequency portion of the spectrum.

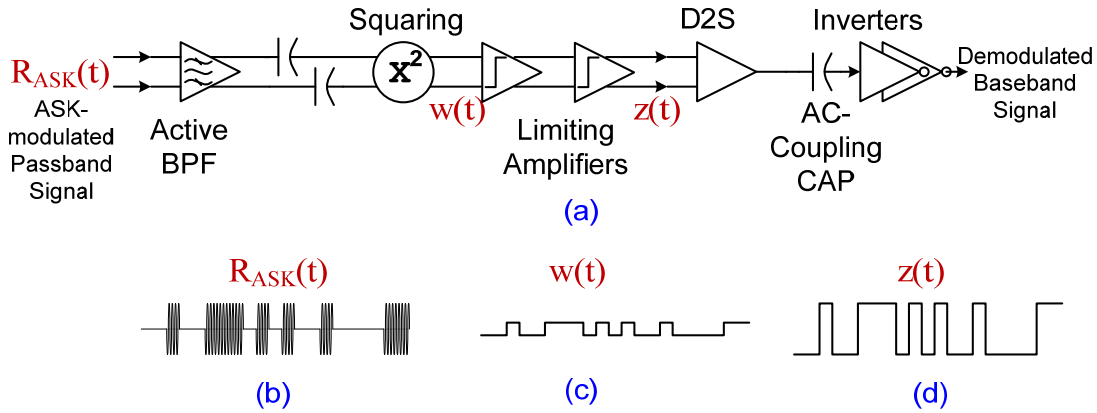


Figure 4-1: (a) Architecture of the non-coherent ASK demodulator; (b) incoming ASK-modulated passband signal; (c) signal waveform at the output of the squaring function; (d) signal waveform at the output of the limiting amplifiers

4.2.2 Circuit Implementation

The circuits of the individual functional blocks in the non-coherent ASK demodulator are depicted in Figure 4-2 and the corresponding simulation performance specifications are shown in Table 4-1. The active BPF (shown in Figure 4-2(a)) utilizes a LC-tank to have a resonance at the desired center frequency and the additional gain can improve the noise figure of the overall receiver. Figure 4-3(a) shows the frequency response of the active bandpass filter. The squaring function is realized by a double-balanced Gilbert-cell mixer (shown in Figure 4-3(b)), in which the differential LO± and RF± ports are tied together. Two limiting amplifiers are cascaded together to achieve the

overall gain required in the receiver chain and the circuit is shown in Figure 4-3(c). The modified PMOS-load (transistors M3 and M4) differential pair with resistors R1 and R2 makes the differential amplifier more robust against device mismatch in IC fabrication process because the common-mode voltage at the differential outputs (node A) is used to bias the two PMOS's. This is important when two or more of the same limiting amplifier are cascaded because a minor DC offset from one gain stage would be further amplified by the one that follows. A differential–to-singled–ended converter (shown in Figure 4-3(d)) is connected to the output of the second limiting amplifier before the AC-coupling capacitor and the analog inverter chain. Figure 4-3(b) and (c) show the simulated P_{1dB} and frequency response of the limiting amplifiers with the differential-to-single-ended converter respectively. The analog inverter consists of a NMOS-PMOS pair with their gates and drains tied together. Their widths determine the turn-on or switch-on DC voltage at the input (gates), which should be the mid-point of the rail-to-rail voltage supply for the best switching performance. All analog inverters draw current from a 1 V power supply instead of the 1.8V power supply used by other blocks.

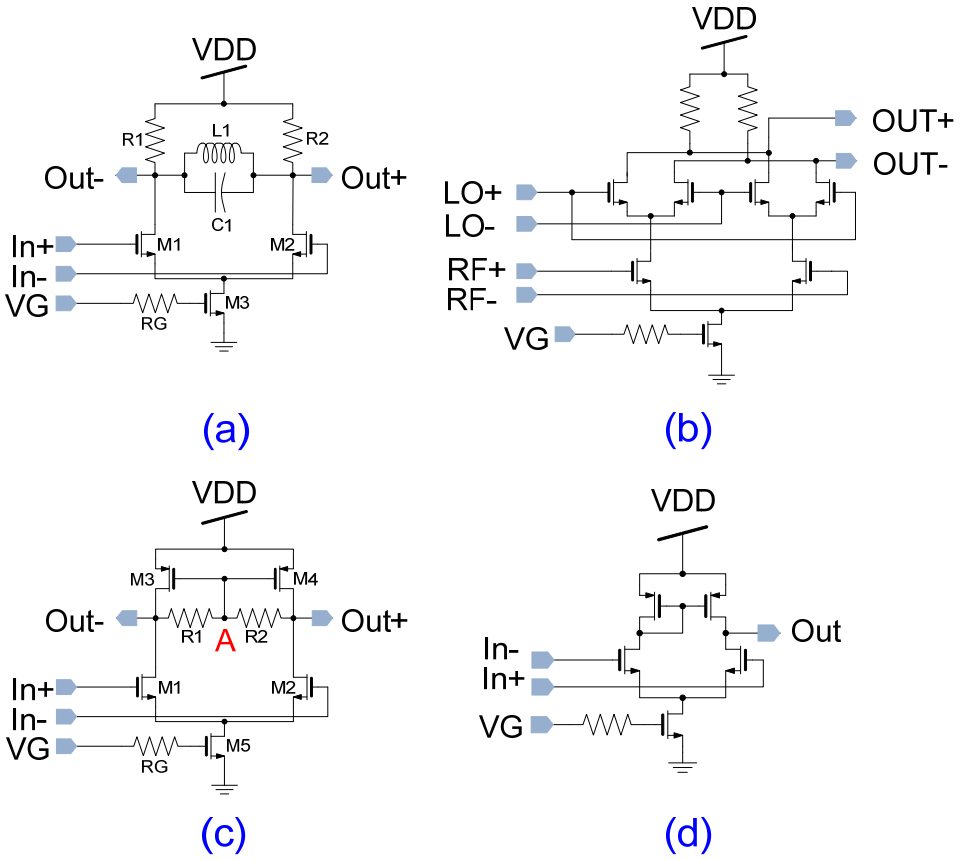


Figure 4-2: (a) Active BPF filter; (b) Gilbert-cell mixer used as a squaring function; (c) limiting amplifier; (d) differential-to-single-ended converter (D2S)

Table 4-1: Simulation performance of the functional blocks of the non-coherent ASK demodulator

Active Bandpass Filter		**Mixer as Squaring**		**Limiting Amplifiers+D2S**	
Gain	6 dB	**Conversion Loss**	27 dB @ -23 dBm	**Gain**	35 dB
Power Consumption	7 mW (1.8 V)	**Power Consumption**	5.5 mW (1.8 V)	**Power Consumption**	22 mW (1.8 V)
Double Sideband Bandwidth	1.25 GHz			**Bandwidth**	1 GHz
Center Frequency	9.2 GHz			**Input P_{1dB}**	20 mVpp

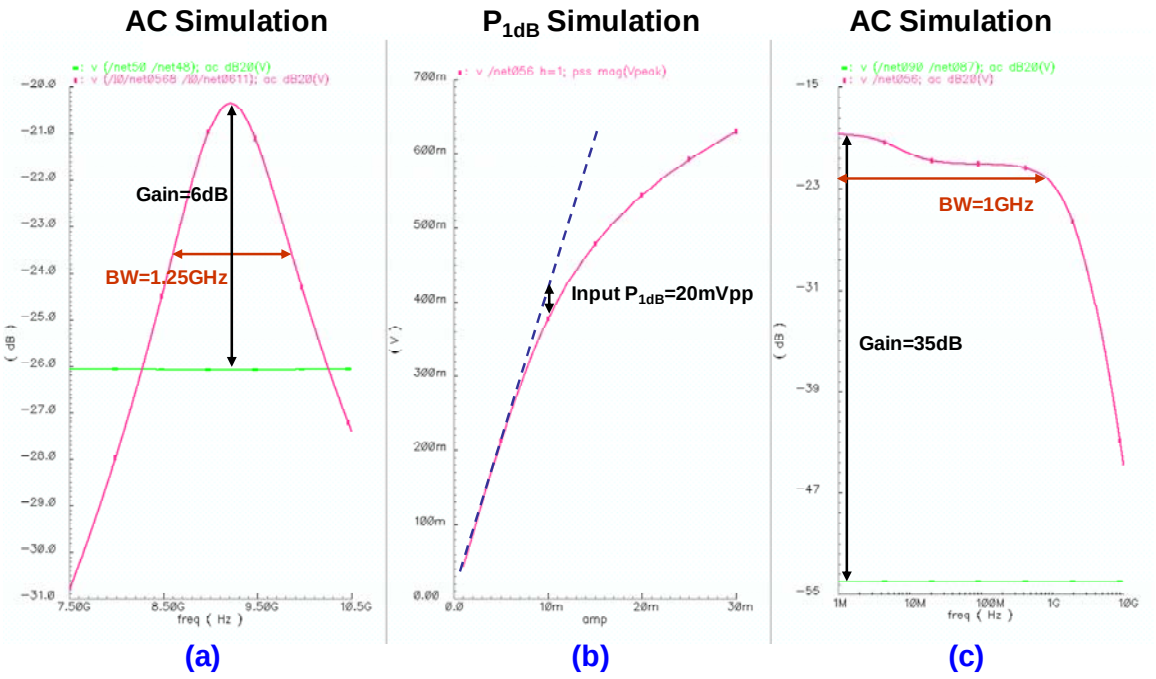


Figure 4-3: (a) Simulated frequency response of the active BPF filter; (b) linearity simulation of the limiting amplifiers with the differential-to-single-ended converter; (c) simulated frequency response of the limiting amplifiers with the differential-to-single-ended converter

4.2.3 Measurement Setup

The ASK measurement setup is shown in Figure 4-4 with the red portion indicating the designed and fabricated multi-gigabit demodulator. This setup can be used to perform both ASK and BPSK multi-gigabit measurement using the amplitude settings of the pulse pattern generator: high threshold = +A / low threshold = -A for BPSK and high threshold = +A / low threshold << A for ASK. The Hittite evaluation board functions as a quadrature up-converter with the digital bitstream modulating the carrier from a LO source. A 180°-hybrid acts as a balun that converts the singled-ended signal into differential inputs to the demodulator under test (DUT). The demodulated baseband

signal from the DUT is then feed into the signal integrity analyzer which analyzes the eye-diagram or the pulse-pattern receiver for bit-error rate (BER) measurement. For high-speed HDMI video streaming demonstration, the demodulated data output is connected to a video-signal converter.

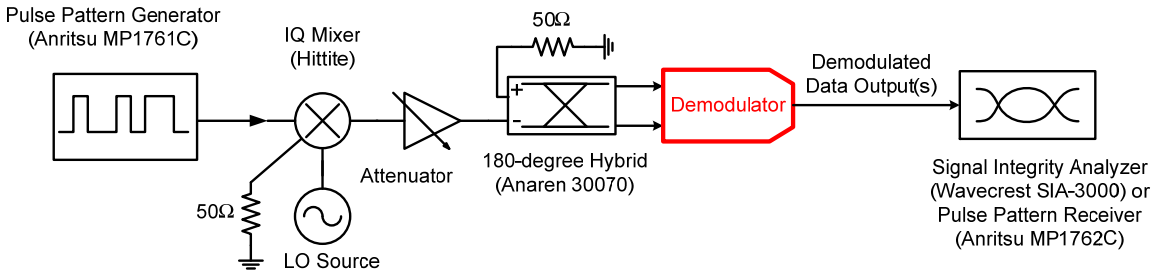


Figure 4-4: Measurement setup of the multi-gigabit demodulator

4.2.4 Performance Evaluation

The non-coherent multi-gigabit ASK demodulator is fabricated in 90 nm CMOS process and a photo of the die is shown in Figure 4-5(a). The overall chip-space is merely 0.9 mm × 0.23 mm without bonding pads. In order to measure its performance, a separate test module (shown in Figure 4-5(b)) is also fabricated using FR-4 for chip mounting and wire-bonding of the IC. The test module gives external access to all I/O and DC control pads.

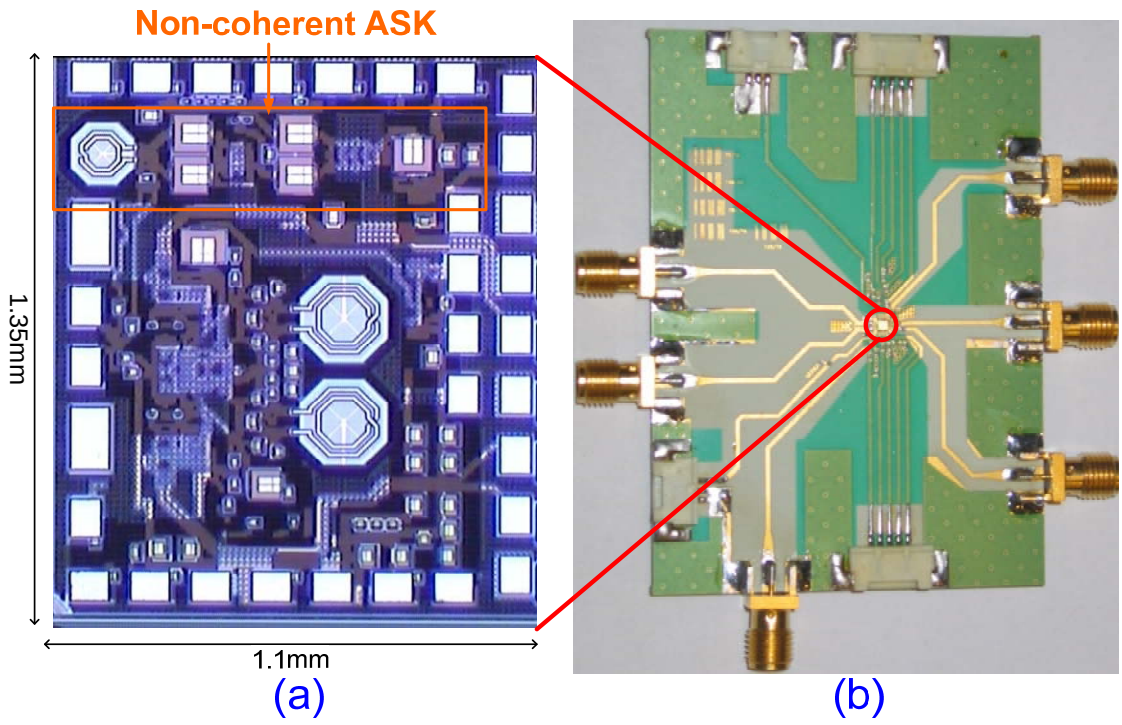
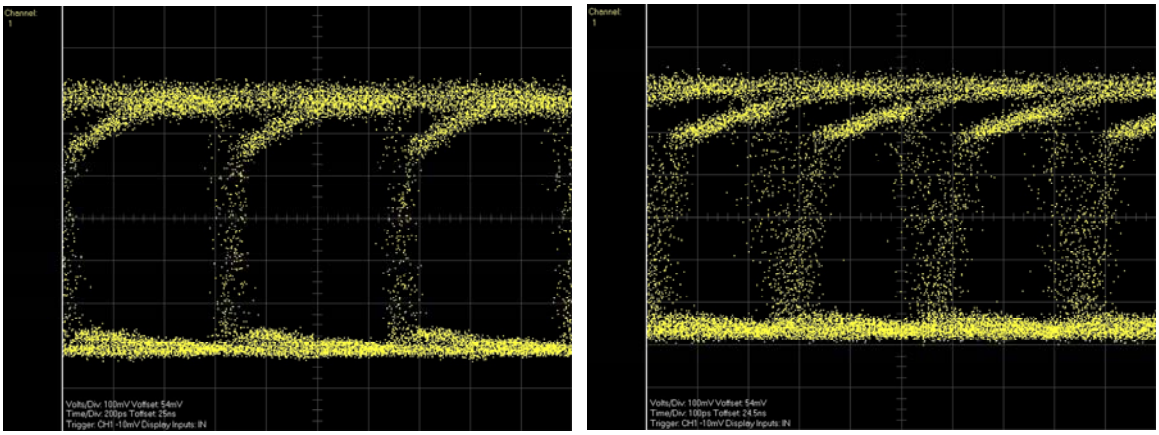


Figure 4-5: (a) Photo of the fabricated non-coherent multi-gigabit ASK demodulator; (b) the FR4 test module for measurement

Table 4-2 provides a performance summary of the non-coherent multi-gigabit ASK demodulation in comparison to the simulation results. It is shown that the measured and simulated performance matches relatively well with each other. The discrepancy between the measured and simulated minimum sensitivity numbers is a result of the parasitic loss from the fabrication process. Figure 4-6(a) shows the measured eye-diagrams of a demodulated signal at error-free 1.5 Gbps transmission at -8 dBm and Figure 4-6(b) shows the measured eye-diagram of a 3.5 Gbps transmission at 0 dBm with BER=4×10^{-8}. Higher speed data transmission requires higher minimum sensitivity as the width of the eye-opening reduces and more error bits are shown in the middle of the eye-diagram.

Table 4-2: Performance summary of the non-coherent ASK demodulator

	Simulation	Measurement
DC Power Consumption	34 mW from 1.8 V	32 mW from 1.8 V
Dynamic Range	23 dB	20 dB
Maximum Speed	3.5 Gbps	≥3 Gbps
Minimum Sensitivity	-26 dBm @ 1.5 Gbps	-20 dBm @ 1.5 Gbps
Operating Frequency Range	6 GHz~10 GHz	6 GHz~9.5 GHz



(a) (b)

Figure 4-6: (a) Eye-diagram of the non-coherent ASK demodulation at 1.5 Gbps, carrier frequency of 9 GHz, signal power of -8 dBm, error-free; (b) eye-diagram of the non-coherent ASK demodulation at 3.5 Gbps, carrier frequency of 9.25 GHz, signal power of 0dBm, measured BER=4×10^{-8}

4.3 Non-Coherent ASK/DBPSK Demodulator

The non-coherent multi-gigabit ASK demodulator discussed in Section 4.2 shows great potentials for simple low-power multi-gigabit wireless applications when the minimum sensitivity requirement is not rigorous. In order to accommodate more

sophisticated devices with better minimum sensitivity and more robustness against RF channel impairment, popular architectures such as the one shown in Figure 4-7 can be used. Such architecture has proven to be versatile and reliable in a today's wireless receiver design. It is also compatible to a typical digital modem design such as OFDM and QAM systems with additional ADCs and DSP for demodulation. However, the proposed non-coherent ASK/DBPSK multi-gigabit demodulator does not require these aforementioned components (ADCs and DSP) to operate. In fact, it is based on the same 1V quadrature analog front-end discussed in Section 3.5 with only few additional circuits (indicated as the ASP) hence it still operates at a minimum power budget without significant performance degradation in either analog or ASK/DBPSK demodulation mode. In addition, the demodulator can be easily integrated into a traditional digital modem design if desired because of its compact size. In such case, one system designer does not need to make any compromise to obtain the ASK/DBPSK demodulation capability when using such architecture. The demodulation technique utilizes the summation of the squared in-phase and quadrature-phase signals in the quadrature analog front-end, called "I^2+Q^2" computation and this is detailed in Section 4.3.1 and Section 4.3.2.

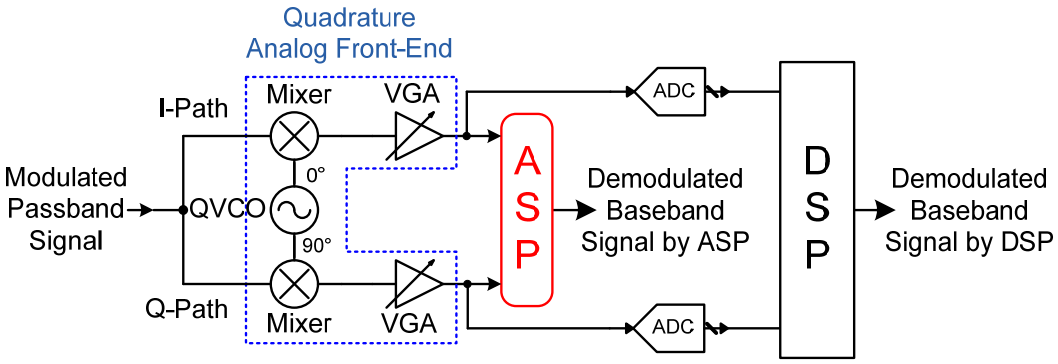


Figure 4-7: Simplified block diagram of the multi-gigabit ASK/DBPSK demodulator

4.3.1 Theory of ASK Demodulation

Figure 4-8(a) and (b) show the original digital bitstream and the ASK-modulated RF carrier respectively. Without frequency and phase synchronization, the down-converted in-phase and quadrature-phase signals appear as in Figure 4-8(c) and the squared version of themselves are shown in Figure 4-8(d). The red dashed line indicates the envelope of a minor frequency difference between the transmitter and receiver local oscillators. Summation of the squared quadrature signals is shown in Figure 4-8(e), which resembles the original data stream. The small wiggling on top of the signal waveform can be smoothed out by limiting amplifiers. Hence, the I^2+Q^2 computation functions as a power detector in the case of ASK demodulation and it shows the same result as the previous ASK demodulator shown in Section 4.2.

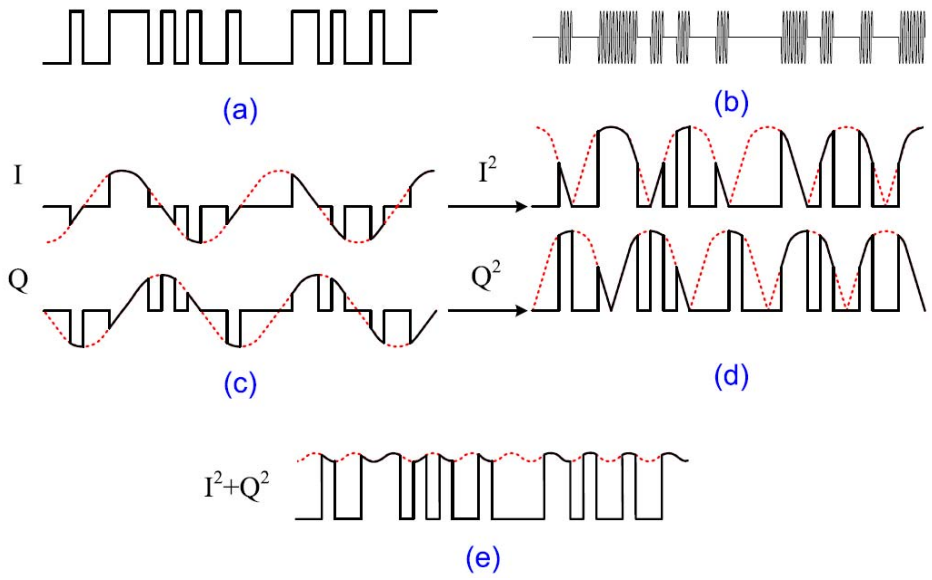


Figure 4-8: Illustration of ASK demodulation using the I^2+Q^2 architecture: (a) the data bitstream in the digital form; (b) the ASK-modulated passband signal; (c) the down-converted in-phase and quadrature-phase baseband signals with frequency offset; (d) squaring of the quadrature signals in (c); (e) summation of the quadrature signals in (d)

4.3.2 Theory of DBPSK Demodulation

On the other hand, the DBPSK demodulation is accomplished using the same I^2+Q^2 computation with minor adjustment. D-BPSK stands for differentially-coded BPSK modulation. The BPSK demodulation is illustrated in Figure 4-9 and the need for differential encoding is shown later in Figure 4-11. Figure 4-9(a) and Figure 4-9(b) shows the original data stream and the BPSK-modulated RF carrier respectively. The down-converted in-phase and quadrature-phase signals with minor frequency offset are shown in Figure 4-9(c). It should be noted that the difference between these down-converted signals in the cases of ASK-demodulation and BPSK-demodulation. Squared signals of Figure 4-9(c) are shown in Figure 4-9(d) without any carrier recovery system. Summation of the quadrature signals in Figure 4-9(d) is shown in Figure 4-9(e) and one can notice that the I^2+Q^2 computation becomes an edge-detector with a BPSK-modulated carrier as the input. Full rail-to-rail signal of Figure 4-9(f) is achieved through limiting amplifiers. In order to recover the original data stream using these edge-detected results, a toggle flip-flop is employed. However, there is a potential ambiguity related to the initial state of a toggle flip-flop (could be either digital "1" or "0") using an edge-detector. The demodulated signal is of the same polarity as the original data stream or of its inverted version as shown in Figure 4-9(g) and Figure 4-9(h) respectively. This polarity ambiguity can be overcome by employing a preamble in front of each data packet transmission.

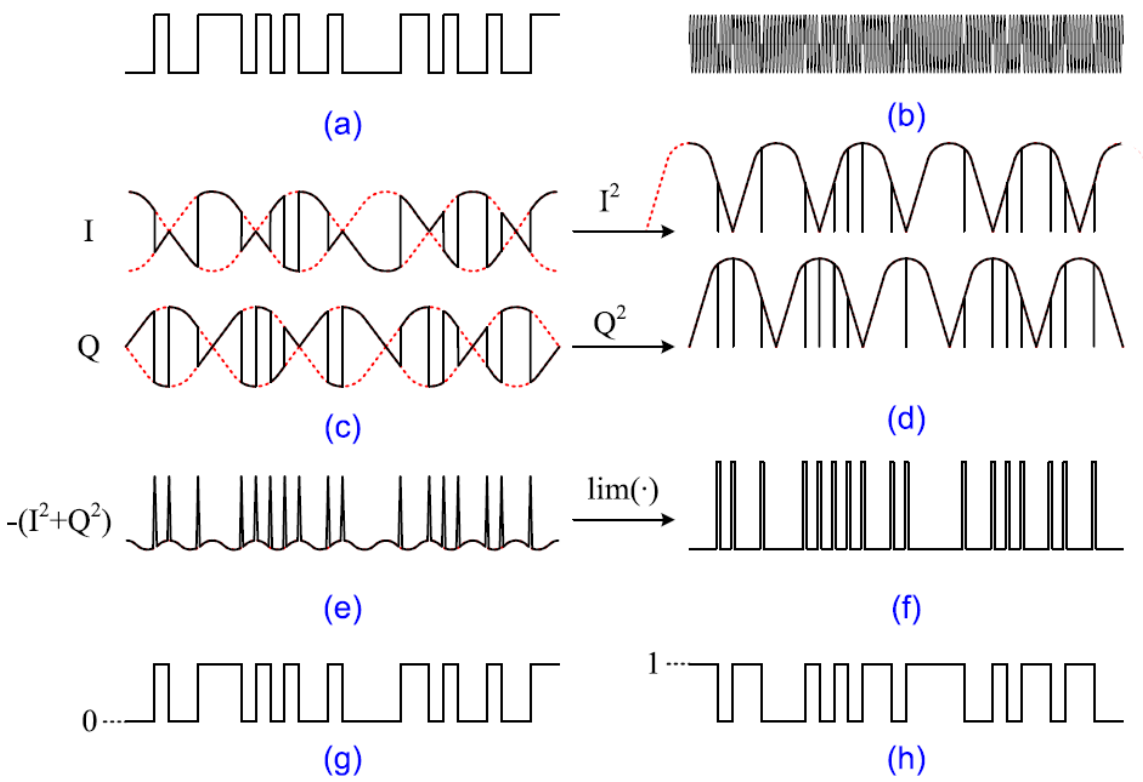


Figure 4-9: Illustration of BPSK-demodulation using the I^2+Q^2 architecture: (a) the data stream in the digital form; (b) the BPSK-modulated passband RF signal; (c) the down-converted quadrature baseband signals with frequency offset; (d) squaring of the quadrature signals in (c); (e) inverted-summation of the inverted quadrature signals in (d); (f) signal in (d) passing through the limiting function; (g) the output of the toggle flip-flop with the input signal of (f) and an initialization of "0"; and (h) the output of toggle the flip-flop with the input signal of (f) and an initialization of "1"

While using the I^2+Q^2 architecture for BPSK demodulation, special attention is required for processing the demodulated signal in a noisy wireless channel. Due to the characteristic of the edge-detection system, one single bit error (i.e. missing edge) results in subsequent erroneous bit-inversion until the next occurrence of a bit error. This condition is illustrated in Figure 4-10(a) where Y(t) is the edge-detected signal using a I^2+Q^2 architecture and Z(t) is the output of the toggle flip-flop, i.e. recovered datastream.

It is shown that the first missing bit of Y(t), circled in red, causes a logic inversion in Z(t) until the next erroneous bit occurs. This results in incorrect (inverted) bit patterns in between two uncorrelated occurrences of bit error and it dramatically impacts the bit-error-rate (BER) performance of the BPSK demodulator. In order to operate a robust communication system against inevitable noisy channel, differential coding scheme ("0" for no change 0→0/1→1 and "1" for 0→1/1→0 changes) could be employed with the I^2+Q^2 edge detection architecture. As illustrated in Figure 4-10(b), DX(t) is the differentially encoded signal of X(t) and it is the actual signal being transmitted over the wireless medium. DY'(t) is the received edge-detected signal with two indicated bit-errors while DZ'(t) is the output signal of the toggle flip-flop. The final differential decoded data stream, DW'(t), only shows the two single bit errors rather than consecutive bit-errors in the non-differential-encoded case. Hence, it has been demonstrated that the BER performance of the BPSK demodulator can be significantly improved by means of differential coding when the I^2+Q^2 architecture is used for demodulation.

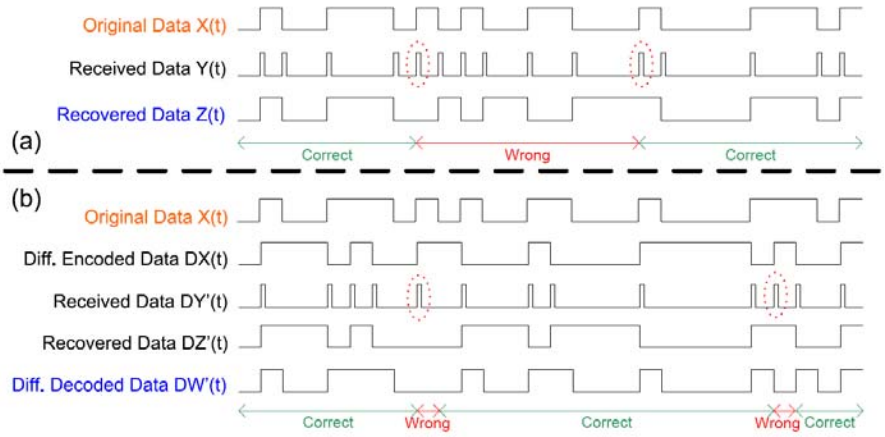


Figure 4-10: Illustration of differential encoding and decoding for the BPSK demodulation using the I^2+Q^2 architecture: (a) without differential-encoding, i.e. standard BPSK and (b) with differential encoding and decoding

4.3.3 Architecture

The architecture of the non-coherent multi-gigabit ASK/DBPSK demodulator is shown in Figure 4-11. It consists of the quadrature analog front-end and the ASP with both sharing the I^2+Q^2 computation result. An integrated PLL is also implemented to control the oscillation frequency of the QVCO. While using in the analog front-end, the I^2+Q^2 circuit produces the integrated baseband signal power for the AGC system as discussed in Section 3.3.2. At the same time, the non-coherent ASK/DBPSK demodulation can be achieved without any interference to the AGC operation. This is due to the application of D2S delivering the power-detector output as well as acting as a buffer between the I^2+Q^2 circuit and the AGC feedback system. While a much slower response (<MHz) is needed for the AGC control loop, a higher bandwidth requirement (>GHz) is essential for the multi-gigabit signal path. The differential amplifier followed by the AC-coupled comparator provides the limiting operation to the ASK/DBPSK demodulated signal and ensures a rail-to-rail digital signal, which can be further processed by the standard digital cells of a given CMOS process. AC-coupling is needed to make the multi-gigabit demodulator more robust against device mismatch and process variation. The toggle flip-flop consists of a D-flip-flop with an inverter.

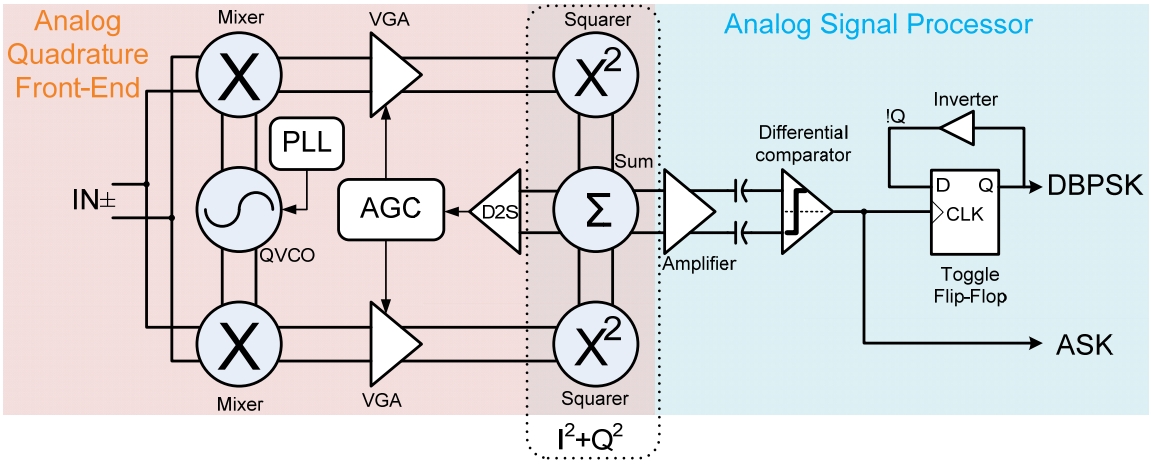


Figure 4-11: Architecture of the multi-gigabit ASK/DBPSK demodulator

4.3.4 Circuit Implementation

Circuit schematics of the I^2+Q^2 circuit and the differential amplifier of the ASP are shown in Figure 4-12(a) and Figure 4-12(b) respectively. As shown in Section 3.2.2, the power-detector circuit of the AGC computes the baseband signal power using the summation result of the squared in-phase and quadrature-phase signals. Hence the same circuit is shared by both the quadrature analog front-end and the non-coherent ASK/DBPSK demodulator. At the output of the differential amplifier, there are two 10 pF on-chip AC-coupling capacitors. In order to drive such large loading, the RC-degeneration broadband technique is employed to maintain the bandwidth along the demodulated signal path. The differential amplifier provides a gain of 3 dB with a 3-dB bandwidth of 2.7 GHz with the capacitor loading and it consumes 4.7 mA from a 1 V power supply.

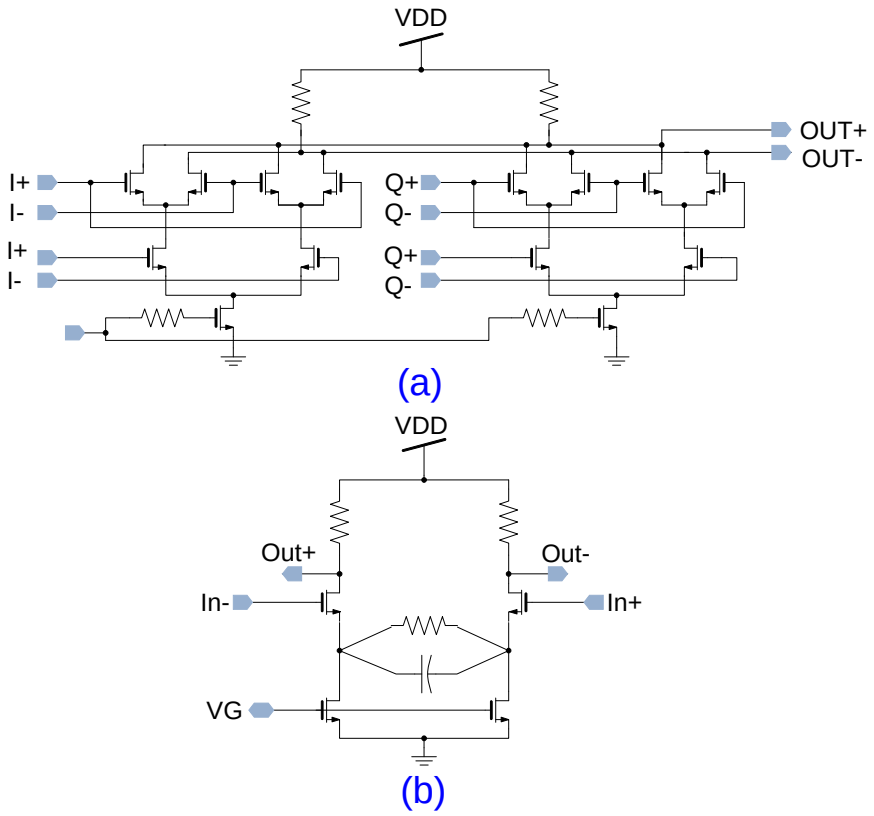


Figure 4-12: Circuit schematic of (a) the I^2+Q^2 circuit and (b) differential amplifier

4.3.4.1 ***Differential Comparator***

The main purpose of the differential comparator is to perform a limiting function to the input signal, either as the demodulated signal when operating as the ASK demodulator or as the edge-detected signal in the case of a DBPSK demodulator. The circuit schematic of the differential comparator is shown in Figure 4-13. It consists of a two-stage PMOS differential-pair amplifier with a cross-coupled load at the first stage and digital inverters from the standard digital cell library at the output [36]. Transistors, M1 and M4 act as positive resistors. On the hand, the cross-coupled transistors, M2 and M3 act as negative resistors. Therefore they cancel each other out to result in high

differential output impedance and relatively high differential gain compared to a standard differential amplifier. The other advantage of such circuit is the inherent common-mode feedback provided by the cross-coupled transistors (M2 and M3). They are diode-connected transistors hence it sets the DC voltage of the first stage output at one V_{GS} above the ground potential. At the output of the second gain stage, digital inverters are used to condition the signal and function as the interface so that any following processing can be performed in the digital domain. Table 4-3 shows the simulated performance of the differential comparator.

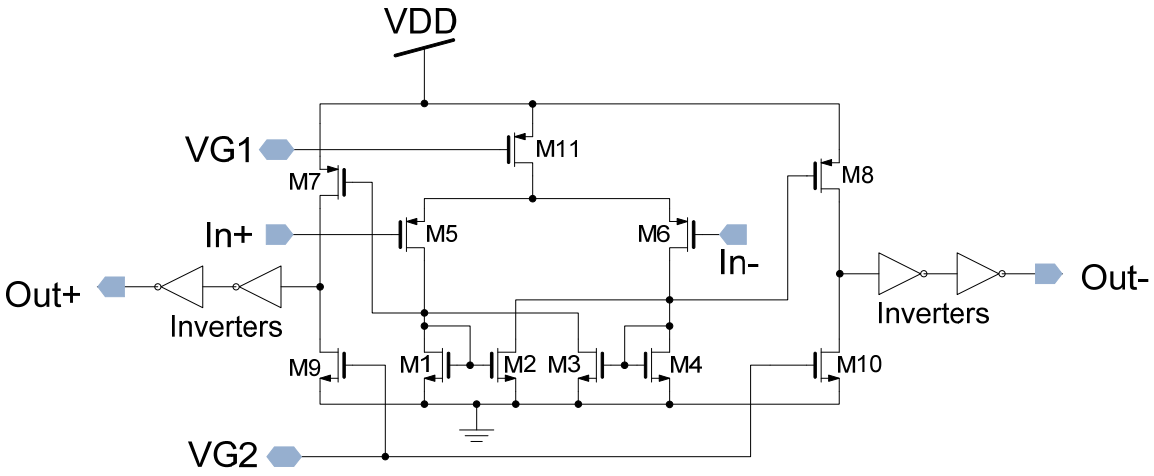


Figure 4-13: Circuit schematic of the differential comparator

Table 4-3: Simulation performance of the differential comparator

Bandwidth	3 GHz
Gain	20 dB
Power Consumption	2.8 mW@1 V
Minimum Sensitivity	50 mVpp Differential

4.3.5 Performance Evaluation

The micrograph of the analog quadrature front-end with the integrated ASKS/DBPSK analog signal processor and its test module are shown in Figure 4-14. The overall size is 1.3 mm × 1.2 mm including all bonding pads although the actual system of interest occupies an area of 0.7 mm × 0.6 mm. The chip is designed and fabricated using standard 90 nm CMOS process. As seen from Figure 4-14, the compact layout allows sufficient room for higher-level integration of additional ADCs and DSPs if desired. The same measurement setup is used as in Section 4.2.3.

Table 4-4 shows the measured and simulated performance summary of the non-coherent multi-gigabit ASK demodulator. The total power consumption is 65 mW (including mixers, QVCO, PLL, amplifier, differential comparator, toggle flip-flop and baseband amplifiers with AGC) from a single 1.0 V supply. However, only 7.5 mW out of the 65 mW is specifically used for ASK demodulation (differential comparator and the preceding RC-degenerative amplifier) as the rest of power consumption comes from the normal operation of the quadrature analog front-end. In addition, the minimum sensitivity of the ASK demodulator is about -40 dBm and it increases with rising data speed. A maximum raw speed of 2.5 Gbps with ASK-modulated signal has been demonstrated without any carrier phase and frequency synchronization. The tolerance of such LO frequency offset is more than ±500 MHz.

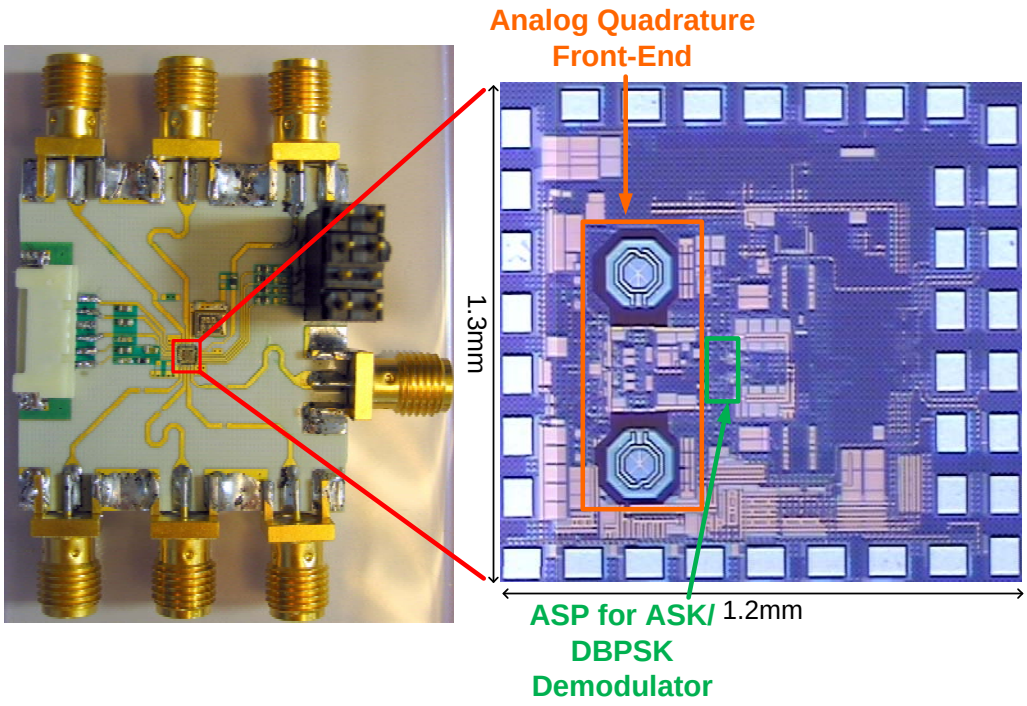


Figure 4-14: (right) Micrograph of the fabricated analog quadrature front-end with built-in ASK/DBPSK multi-gigabit demodulator; (left) test module used for measurement

Table 4-4: Performance summary of the non-coherent ASK demodulator

	Simulation	**Measurement**
Operating Range	More than ±500 MHz	More than ±500 MHz
Minimum Sensitivity	-42 dBm @ 2 Gbps	-38 dBm @ 1.485 Gbps -42 dBm @ 0.864 Gbps
Dynamic Range	11 dB without AGC	32 dB with AGC
DC Power Consumption	64 mW @ 1 V	65 mW @ 1 V

Under several different data transmission speeds, the measured BER at various input power of the ASK-modulated IF carrier is shown in Figure 4-15. The measured eye-diagrams are shown in Figure 4-16 for speeds at 0.864 Gbps, 1.5 Gbps, 2 Gbps and

2.5 Gbps. A separate HDTV streaming experiment has also been performed and it demonstrates the potential capability of this multi-gigabit demodulator.

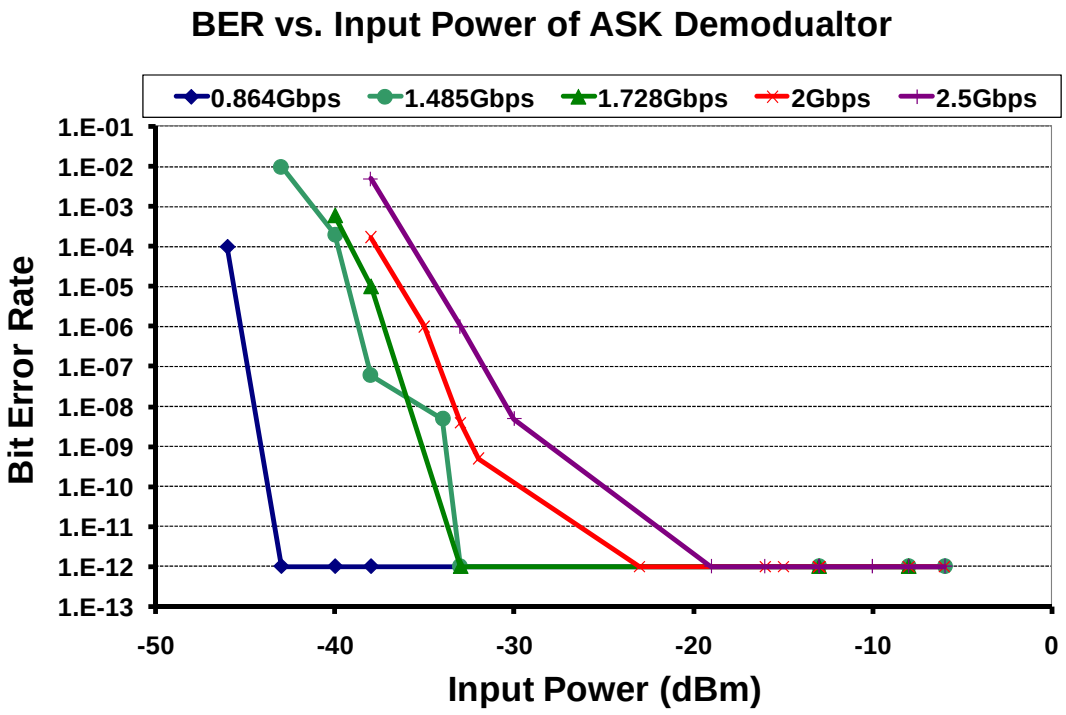


Figure 4-15: Measured BER at various input power of the ASK-modulated IF carrier at 0.864 Gbps, 1.485 Gbps, 1.728 Gbps, 2 Gbps and 2.5 Gbps

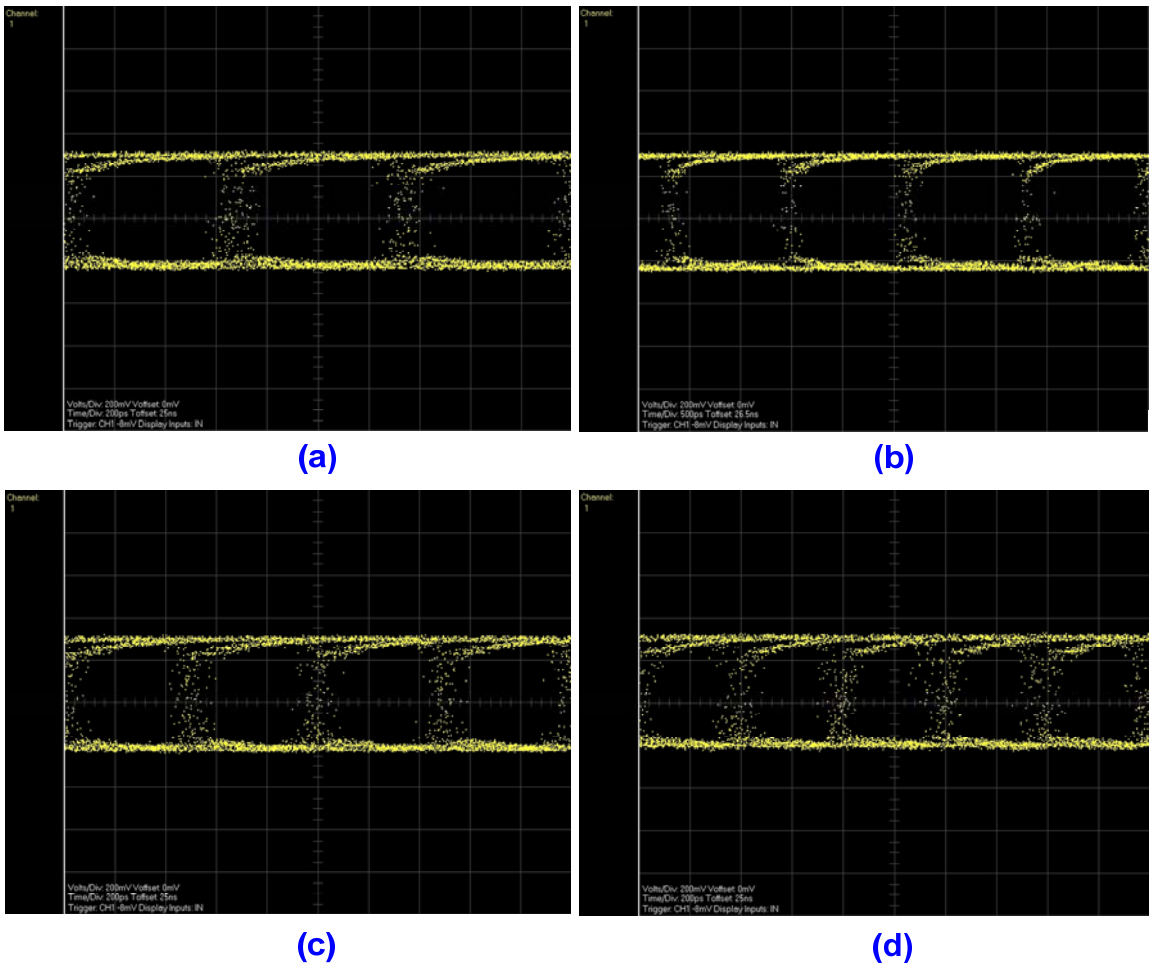


Figure 4-16: Measured eye-diagrams of the non-coherent ASK demodulator: (a) IF=-40 dBm at 0.864 Gbps, error-free; (b) IF=-32 dBm at 1.5 Gbps, error-free; (c) IF=-31 dBm at 2 Gbps, BER=1E-9; and (d) IF=-25 dBm at 2.5 Gbps, BER=1E-9

As for the DBPSK demodulation measurement, its performance could not be fully characterized due to the vulnerability and susceptibility of the edge-detection system to the inevitable DC offset within the differential signal path. The similar DC offset also exists in the ASK demodulator signal but its effect does not have significant impact on its performance. Furthermore, the bandwidth requirement for the DBPSK demodulator has to be doubled in comparison to the ASK operation. This is a result from the squaring of the baseband modulated signal, in which the edge-detected signals contains components

of twice the maximum frequency content of the original data stream. In theory, the maximum operating data speed of the non-coherent DBPSK operation is approximately half of that the ASK can achieve. However, a measured eye-diagram of 1 Gbps DBPSK demodulated signal is shown in Figure 4-17. It proves that a quadrature analog front-end with improved robustness against DC offset can efficiently demodulate DBPSK signal without the needs of sophisticated carrier phase and frequency recovery system.

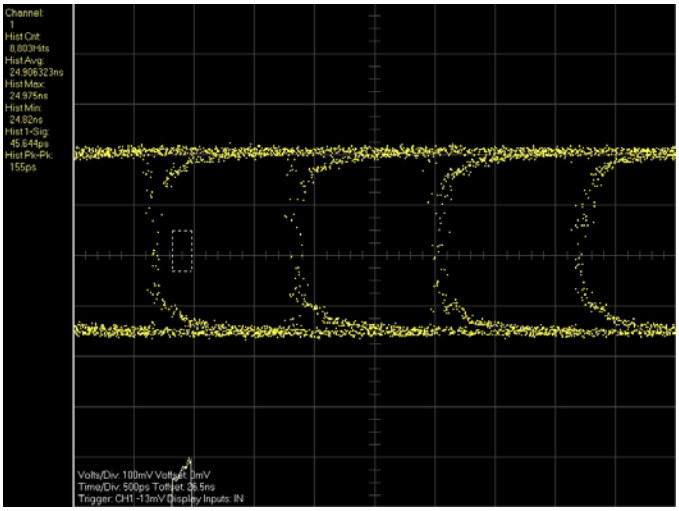


Figure 4-17: Measured eye-diagrams of the non-coherent DBPSK demodulator: IF=-20 dBm at 1 Gbps, BER=1E-9

4.4 Summary

In this section, two different non-coherent demodulator architectures are proposed and demonstrated based on analog signal processing techniques and they provide low-power multi-gigabit demodulation alternatives to the traditional ADC and DSP approaches. Table 4-5 provides a comparison of the performance specifications between them. The first ASK-demodulator (from Section 4.2) can achieve a maximum

transmission speed of 3 Gbps at merely 32 mW of DC power consumption. However, the poor sensitivity (almost 20 dB lower) and inflexible architecture limits its use to low-power and simple best-of-effort type of applications.

Table 4-5: Performance comparison of the non-coherent multi-gigabit ASK demodulators

	Section 4.2	**Section 4.3 (I^2+Q^2)**
Maximum Speed	3 Gbps	2.5 Gbps
Minimum Sensitivity	-20 dBm @ 1.5 Gbps	-38 dBm @ 1.5 Gbps
Frequency Offset Tolerance	More than ±500 MHz	More than ±500 MHz
Dynamic Range	20 dB	32 dB
DC Power Consumption	32 mW @ 1.8 V	65 mW @ 1 V only 7.5 mW for demodulation
Efficiency	10.67 pJ/bit	3 pJ/bit

On the other hand, the I^2+Q^2 ASK demodulator consists of a versatile architecture that is compatible to the standard quadrature receiver design (with additional ADCs and DSP). The higher sensitivity makes it perfect for more advanced applications when a superior receiver performance is required. In addition, the maximum speed can be easily increased by improving the baseband bandwidth of the analog quadrature front-end. While the overall DC power consumption is 65 mW, only 7.5 mW is dedicated for the analog signal processing during the demodulation process. To the best of the author's knowledge, the 3 pJ/bit efficiency of such ASK demodulator is the lowest number that is ever reported by any published literatures and commercial products.

Chapter V

Coherent Demodulator

5.1 Introduction

Although the non-coherent demodulator can recover the original transmitted multi-gigabit digital bitstream without any carrier recovery mechanism, it has done so with a lower minimum sensitivity. On the other hand, a coherent demodulator performs the phase estimation in the receiver and generates a LO signal that is quasi-synchronizing to the transmitter's counterpart. Hence, the wireless receiver can correct the carrier-phase offset in the received signal caused by the propagation delay or a frequency-selective fading channel. In this chapter, the focus is on the design and implementation of the carrier-recovery circuitry for demodulating suppressed-carrier BPSK modulation in the multi-gigabit wireless CMOS receiver. A brief summary of the popular carrier-recovery techniques is provided. Section 5.2 describes the system architecture and circuit implementation details of an ASP for coherent BPSK demodulator. A handover mechanism between the ASP and PLL is presented in Section 5.3. Finally, measurement results of the fabricated multi-gigabit CMOS demodulators are also presented to demonstrate the BER and video streaming performance.

5.1.1 Reviews of Prior Arts

As mentioned in Section 2.4, PSK modulation has better power and bandwidth efficiencies compared to ASK and FSK. In particular, BPSK is the most efficient binary data modulation techniques in terms of noise immunity per unit bandwidth [37]. In this section, two different carrier-recovery approaches for suppressed-carrier BPSK demodulation are discussed in details and their configurations are shown in Figure 5-1.

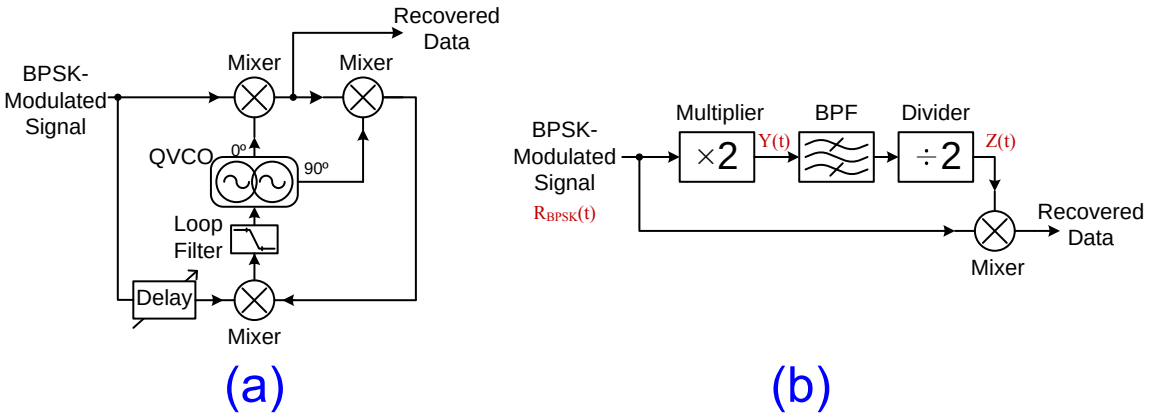


Figure 5-1: Carrier-recovery techniques: (a) remodulator approach; (b) multiply-filter-divide approach

Remodulation is a popular carrier-recovery technique and its functional blocks are shown in Figure 5-1(a). The incoming BPSK-modulated signal is demodulated and the original datastream is recovered. This baseband data is used to remodulate the incoming signal. When the remodulation feedback loop is operating correctly, the original BPSK modulation is completely removed by the recovered carrier which is frequency and phase synchronized with the incoming BPSK-modulated signal. The remodulation loop functions as a PLL that keeps tracking with the carrier. However, the remodulation

technique is typically used in much lower data rates since all operations can be achieved in digital hardware implementation. In addition, it cannot support multiple data rates as a variable time-delay element dramatically impacts the realization of wideband synchronization.

Multiple-filter-divide is another carrier-recovery technique and its main blocks are shown in Figure 5-1(b). This method can be explained mathematically as follow

$$R_{BPSK}(t) = \sin\left[\omega_{BPSK}t + \pi(i-1)\right], \text{ where } i=1,2 \tag{12}$$

$$Y(t) = R_{BPSK}{}^{2}(t) = \sin^{2}[\omega_{BPSK}t + \pi(i-1)] = \frac{1}{2} - \frac{1}{2}\cos\left[2\omega_{BPSK}t + 2\pi(i-1)\right] \tag{13}$$

The squared signal, *Y(t)*, has a frequency components that is twice the modulated carrier frequency with phase zero (modulo 2π). Hence the frequency divider after the BPF can provide a clean carrier, *Z(t)*, that is frequency- and phase-synchronizes with the original received signal. This technique is feedforward in comparison to the feedback loop used by the remodulator. Although the multiply-filter-divide is mathematically simple in theory, said it is not the case when it comes to its practical implementation. Controlling the phase offset is complicated and extremely layout-dependent, in which the recovered carrier takes a completely different signal path from the actual demodulation path. This creates time-delay and phase discrepancy between the receiver LO (i.e. recovered carrier) and the BPSK-modulated signals. In addition, the BPF has to be achieved with multiple filters and it is difficult to maintain a proper phase across a wide operating carrier frequencies.

5.2 Coherent BPSK Demodulation

The third carrier-recovery technique is the Costas loop and the main functional blocks of this implementation are shown in Figure 5-2 [38]. It can be shown that such demodulation is mathematically equivalent to the remodulator [39]. However, it can accommodate multiple data rates unlike the remodulator architecture. The critical benefit of this architecture is its compatibility with the aforementioned analog quadrature front-end in Chapter 3. Without significant impact on the existing critical signal path, a multi-gigabit coherent BPSK demodulator can be easily integrated with the analog front-end. By means of using an ASP that recovers the carrier and simultaneously demodulates the original datastream, there is no need to include the power hungry data-converters and DSP modem(s). Hence, a low-power multi-gigabit demodulator solution can be integrated into CMOS wireless transceiver for ultra-portable applications.

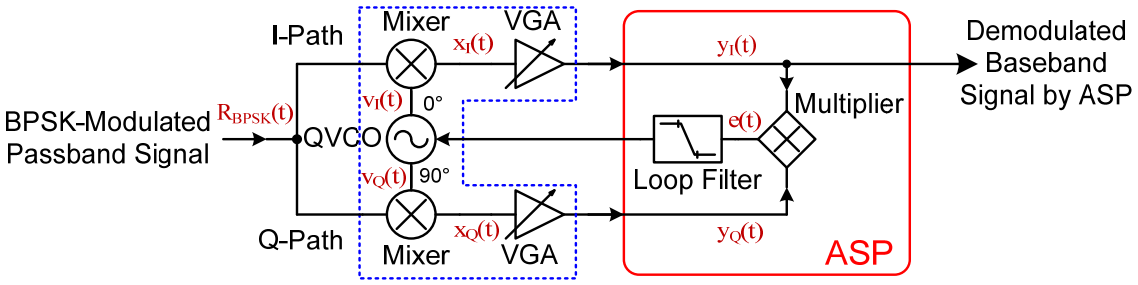


Figure 5-2: The coherent BPSK demodulator using Costas loop as the ASP

The theoretical analysis of the Costas loop is presented in this section. In addition, the system architecture and circuit implementation issues are also detailed. Finally, the measurement results of the fabricated multi-gigabit BPSK demodulator is discussed.

5.2.1 Theory of the Coherent BPSK Demodulation

The operation of the Costas loop can be mathematically demonstrated by the following equations (please refer to Figure 5-2), in which $R_{BPSK}(t)$ is the BPSK-modulated signal, $v_I(t)$ and $v_Q(t)$ represent the quadrature outputs of the VCO with a known phase difference, θ_e [40]

$$R_{BPSK}(t) = D(t)\cos(\omega_{BPSK}t), \text{ where } D(t)=A \text{ for1; } -A \text{ for } 0 \tag{14}$$

$$v_I(t) = \cos(\omega_{VCO}t + \theta_e) \;\&\; v_Q(t) = \sin(\omega_{VCO}t + \theta_e) \tag{15}$$

The down-converted $x_I(t)$ and $x_Q(t)$ are shown below applying the trigonometry

$$\begin{aligned} x_I(t) &= R_{BPSK}(t) \times v_I(t) = D(t)\cos(\omega_{BPSK}t)\cos(\omega_{VCO}t + \theta_e) \\ &= \frac{1}{2}\{\cos[(\omega_{VCO} - \omega_{BPSK})t + \theta_e] + \cos[(\omega_{VCO} + \omega_{BPSK})t + \theta_e]\} \end{aligned} \tag{16}$$

$$\begin{aligned} x_Q(t) &= R_{BPSK}(t) \times v_Q(t) = D(t)\cos(\omega_{BPSK}t)\sin(\omega_{VCO}t + \theta_e) \\ &= \frac{1}{2}\{\sin[(\omega_{VCO} - \omega_{BPSK})t + \theta_e] + \sin[(\omega_{VCO} + \omega_{BPSK})t + \theta_e]\} \end{aligned} \tag{17}$$

The high frequency components, i.e. $\omega_{VCO}+\omega_{BPSK}$, shown in the quadrature baseband signal paths are filtered by the inherent low-pass response of the VGA. With omission of the linear scaling factor from the VGA gain, the multiplication results of the filtered $x_I(t)$ and $x_Q(t)$, i.e. $y_I(t)$ and $y_Q(t)$, produces the error signal, $e(t)$ shown in

$$\begin{aligned} e(t) &= y_I(t) \times y_Q(t) = \cos[(\omega_{VCO} - \omega_{BPSK})t + \theta_e] \times \sin[(\omega_{VCO} - \omega_{BPSK})t + \theta_e] \\ &= \frac{1}{2}\{\sin 0 + \sin[2(\omega_{VCO} - \omega_{BPSK})t + 2\theta_e]\} = \frac{1}{2}\sin\{2[(\omega_{VCO} - \omega_{BPSK})t + \theta_e]\} \end{aligned} \tag{18}$$

By applying the approximation of $\sin\phi \cong \phi$ (for small ϕ), the error signal proved in (18) is proportional to the phase and frequency differences.

$$e(t) = \frac{1}{2}\sin\{2[(\omega_{VCO} - \omega_{BPSK})t + \theta_e]\} \propto (\omega_{VCO} - \omega_{BPSK})t + \theta_e \quad (19)$$

The loop filter following the multiplier removes extraneous multiplication products in *e(t)* before it is applied to QVCO's control using a negative feedback. From the mathematical expressions, the Costas loop can recover the carrier and demodulate the BPSK signal simultaneously.

5.2.2 System Simulation

Although the mathematical equations of the Costas loop are proven in Section 5.2.1, the system-level verification is required to gain better understanding of the overall performance in terms of feedback parameters such as loop gain, loop bandwidth and gain allocation in the signal path. Figure 5-3 shows a Simulink model of the BPSK demodulator created in MATLAB: generation of the BPSK-modulated carrier is shown on the left side of the model and the coherent BPSK demodulator, which resembles the architecture shown in Figure 5-2, is on the right side. The Costas loop is constructed using ideal multipliers for frequency conversion and ideal transfer function and gain blocks for other loop parameters. The Simulink simulation results are shown in Figure 5-4 for the denoted corresponding Simulink scopes.

For the created MATLAB model of the coherent BPSK demodulator, values of the key blocks, namely "VGA_LPF_I", "VGA_LPF_Q", "Loop_Gain", and "Loop_Filter" are carefully determined. "VGA_LPF_I" and "VGA_LPF_I" provides the gain and low-pass filtering to the down-converted quadrature signals. The ideal multiplier

that functions as the phase detector is followed by the “Loop_Gain” and “Loop_Filter” blocks. These two parameters are critical and they are directly related to the synchronization range (also called locking range), dynamic range and stability of the coherent BPSK demodulator. The two “Continuous-Time QVCO” blocks are set to different center-frequencies of oscillation to observe the frequency synchronization capability of the Costas loop. As the loop gain increases, the tolerance of the frequency offset between the two oscillators increases. However, a large loop gain also leads to a higher possibility of instability in the loop as the feedback signal might overshoot to correct the frequency and phase offset. The loop filter bandwidth also contributes to the synchronization range of the coherent BPSK demodulator as a small loop bandwidth results in a stable but lower synchronization range. Therefore, tradeoff between the loop gain and loop filter bandwidth is carefully studied in Simulink to achieve the best compromise and/or combination of these two parameters. Furthermore, the overall gain distribution between the baseband VGA gain and the loop gain has a significant impact on the dynamic range of the Costas loop performance.

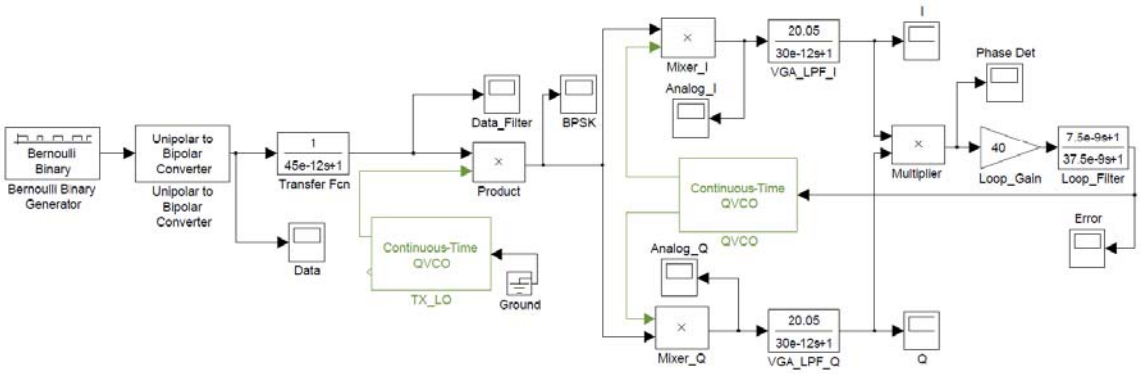


Figure 5-3: MATLAB Simulink model setup of the coherent BPSK demodulator using Costas loop

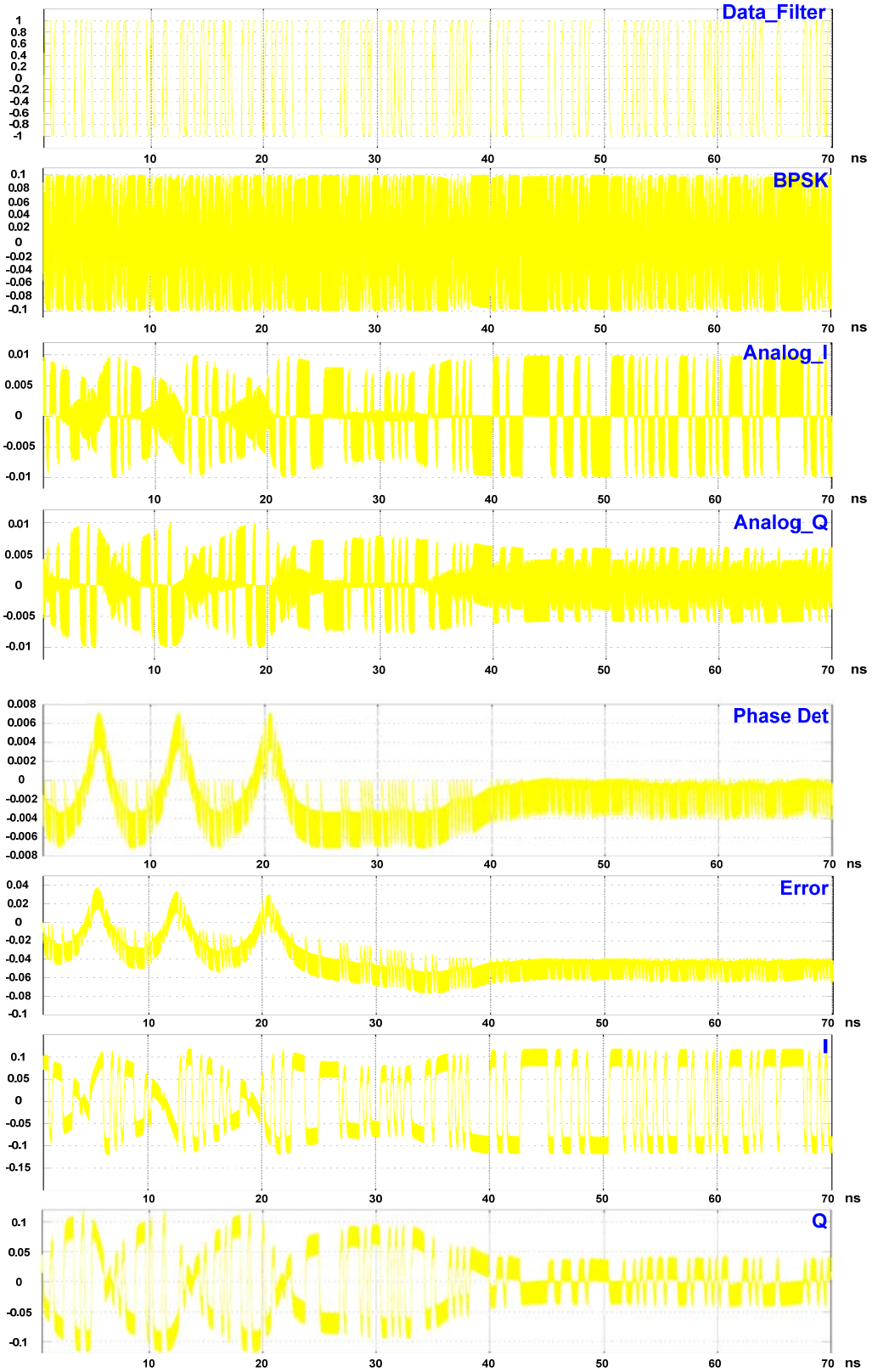


Figure 5-4: MATLAB Simulink simulation results of the coherent BPSK demodulator

The Simulink simulation results shown in Figure 5-4 have a preset frequency offset of 100 MHz between the two oscillators. With K_{VCO}=2 GHz/Volt, the "Error" signal, which directly feeds to the tuning port of the QVCO, finally settles at an average value of -50 mV after approximately 40ns from the start-up of the transient loop response. The time required to achieve the frequency synchronization, also called frequency acquisition time, is a disadvantage of the Costas loop. However, an innovative mechanism is detailed in Section 5.3 and it is shown to help reduce this acquisition time. When the Costas loop is working in a stable condition, the original data stream is recovered in the in-phase channel and a smaller magnitude of that residue is in the quadrature channel.

Although the Simulink model coincides well with the mathematical expression of the Costas loop, the MATLAB is deemed to be too ideal for an actual circuit implementation. Therefore, a co-design approach of both ideal linearized blocks and actual circuits are required in the Cadence Virtuoso environment as shown in Figure 5-5. The respective time-domain transient simulation results are shown in Figure 5-6.

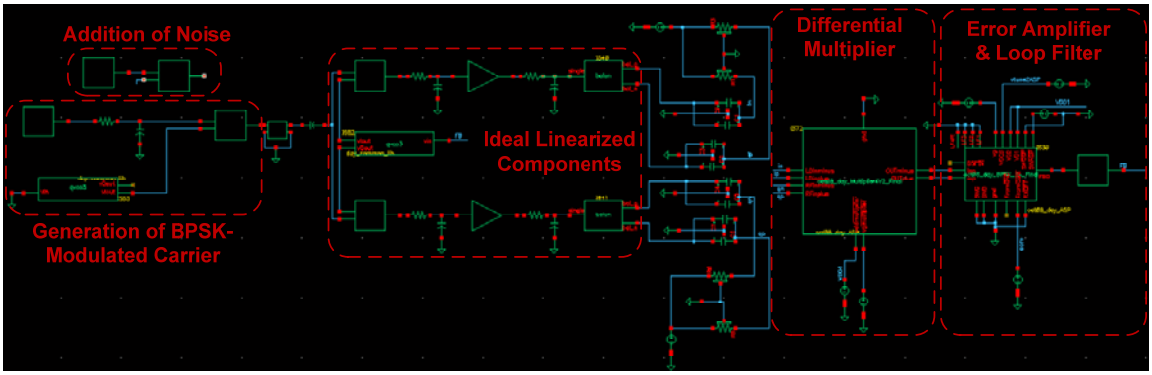


Figure 5-5: Co-design in the Cadence Virtuoso environment involving ideal linear block-level components and transistor-level circuit designs

In the Cadence Virtuoso Schematic, mixers, VGA and QVCO (as well as the components used to generate BPSK-modulated carrier) are approximated by ideal Verilog-A components. Non-linear components, namely the differential multiplier, the error amplifier (corresponds to the loop gain block in Simulink model) and loop filter, are implemented using real circuits from the design kit. The co-design provides a more realistic insight of the Costas loop behavior at a transistor-level implementation. At the same time, it significantly reduces the overall simulation time required to perform a repetitive loop characterization. As shown in Figure 5-6, the coherent BPSK demodulator in the co-design environment provides a similar performance as the MATLAB Simulink simulation results. Furthermore, an AWGN channel (denoted by the addition of noise) can be included in the co-design environment to determine the loop response under a noisy wireless channel. This step helps determine the required SNR for a stable synchronization by the Costas loop as well as the quality of demodulated bitstream (in terms of jitters in the eye-diagram).

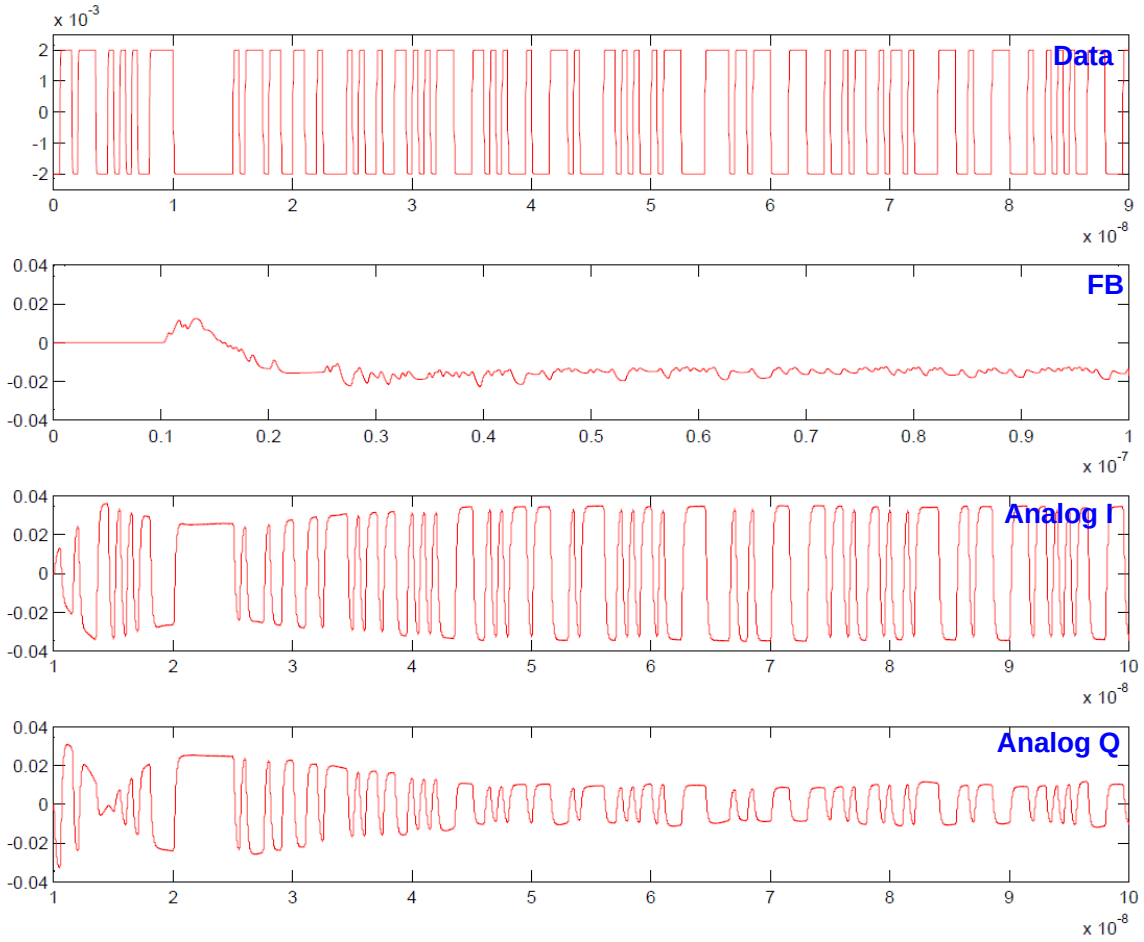


Figure 5-6: Transient simulation results from the co-design Cadence Virtuoso environment

5.2.3 Architecture

The architecture of the coherent multi-gigabit BPSK demodulator is depicted in Figure 5-7. It consists of the 1 V analog quadrature front-end detailed in Section 3 and the ASP using Costas loop for carrier recovery. A differential signal path throughout the system is chosen to increase the overall dynamic range in a 1 V supply voltage. The QVCO is controlled by a feedback signal generated from the ASP. The VGA with a finite cut-off bandwidth functions as the low-pass filter for Costas loop. Within the loop, the

buffer amplifier in front of the on-chip AC-coupling capacitors is required to avoid the large loading of the capacitor in the main signal path. This allows the analog quadrature front-end to provide the available baseband bandwidth especially when optional data converters are used in the traditional demodulation approach. This buffer amplifier is implemented as the RC-degenerated amplifier detailed in Section 3.3.3. The differential multiplier works as a phase detector and its output represents an error signal that is proportional to the minor frequency deviation and phase offset between the receiver's and transmitter's LOs. The error amplifier at the output of the multiplier provides additional loop gain to the error signal and it is followed by the loop filter. The significance of the QVCO buffer is emphasized as it provides an external tuning control of the oscillation frequency as well as an interface between the ASP and the integrated PLL, which is discussed in Section 5.3. Finally, the error signal at the output of the QVCO buffer completes a negative feedback control loop that constantly corrects these frequency drift and phase-offset of the receiver's QVCO to maintain the synchronization. The synchronization criterion helps the demodulation process because of the principle of coherency and orthogonality. The low-frequency mixing product of a BPSK-modulated signal and its coherent carrier is the demodulated baseband information in the I-path. However, the low-frequency mixing product is completely cancelled in the case of a BPSK-modulated signal multiplied by its orthogonal carrier (a carrier that is 90° or $\pi/2$ out of phase with its coherent carrier) in the Q-path. Differential comparator, which is discussed in Section 4.3.4.1, is employed as the limiting amplifier to provide a rail-to-rail digital signal from the recovered analog waveform.

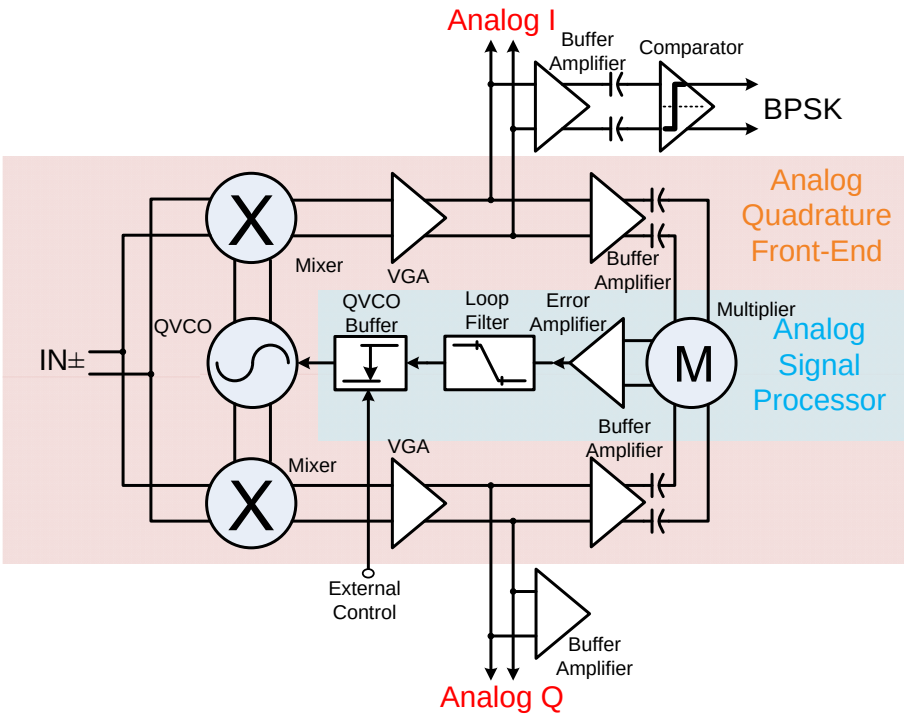


Figure 5-7: Architecture of the coherent BPSK demodulator using Costas loop as the analog signal processor

Figure 5-8 shows the Cadence transient simulation results of the coherent BPSK demodulator using real circuits implemented in the 90 nm CMOS design kit. The waveforms resemble those of the MATLAB Simulink model and it shows the feasibility of such multi-gigabit BPSK demodulator architecture. The recovered bitstream is shown as the inverse polarity of the original bitstream. This phenomenon is due to the phase ambiguity involved in the loop response as both 0º- and 180º-phase of the recovered QVCO carrier are stable conditions. Nevertheless, this is generally resolved by the implementation of a known sequence called, “preamble” in the communication protocol to correct any phase inversion.

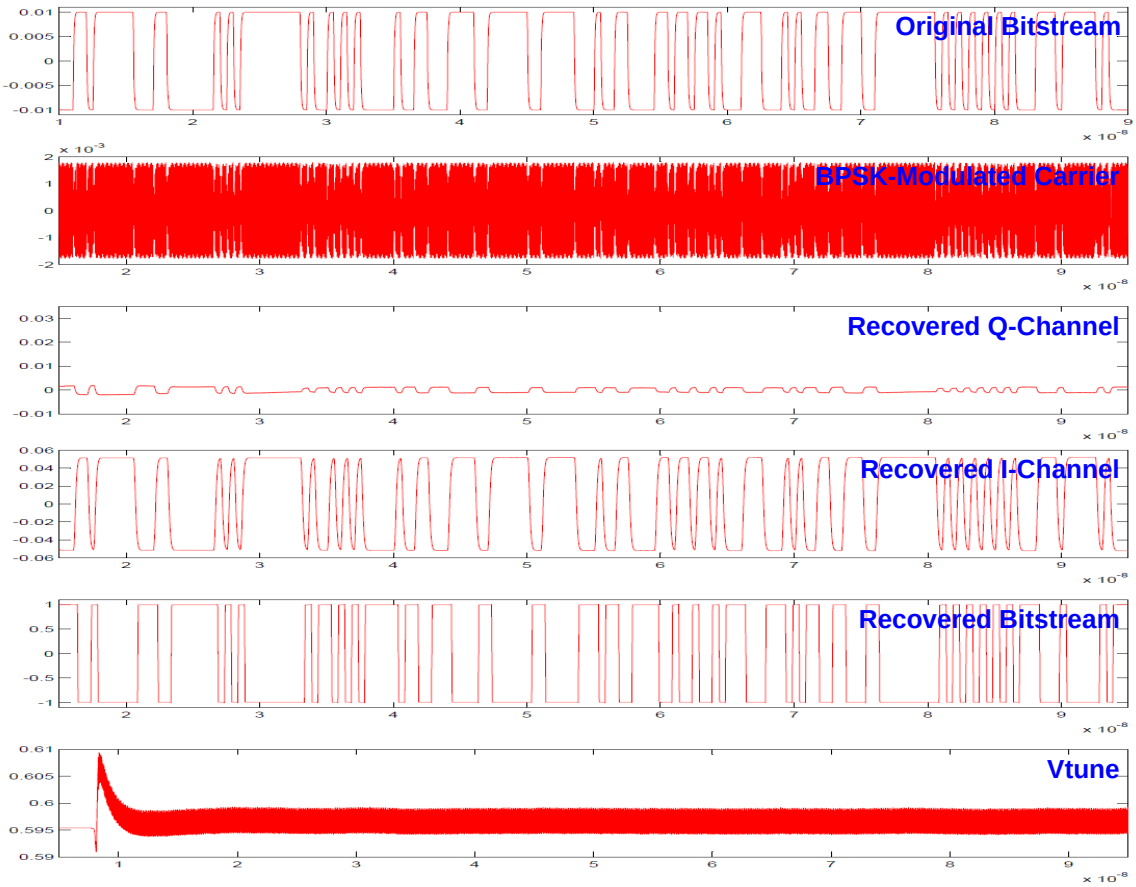


Figure 5-8: Cadence simulation results of the coherent BPSK demodulator using real transistor-level circuits

The previous simulation shown in Figure 5-8 is performed using rectangular pulses with little filtering in effect. In reality, the transmitted rectangular bitstream waveform is passed through a pulse-shaping filter to reduce the occupied spectrum bandwidth and diminish excessive sidelobes in the transmitted spectrum. However, the pulse-shaping filter makes a smoother data pulse transition (0→1/1→0) and it makes the detection of phase-error between I- and Q-channels more difficult. The coherent BPSK-demodulator architecture using Costas loop is robust to operate with the pulse-shaping filtering. Figure 5-9 depicts the Cadence transient simulation results with α=35% raised-

cosine finite-impulse filter (FIR). Although the transmitted BPSK-modulated carrier looks less than ideal in comparison to that in Figure 5-8, the demodulator can still recover the original bitstream with slightly higher noise in the error (shown as Vtune) signal.

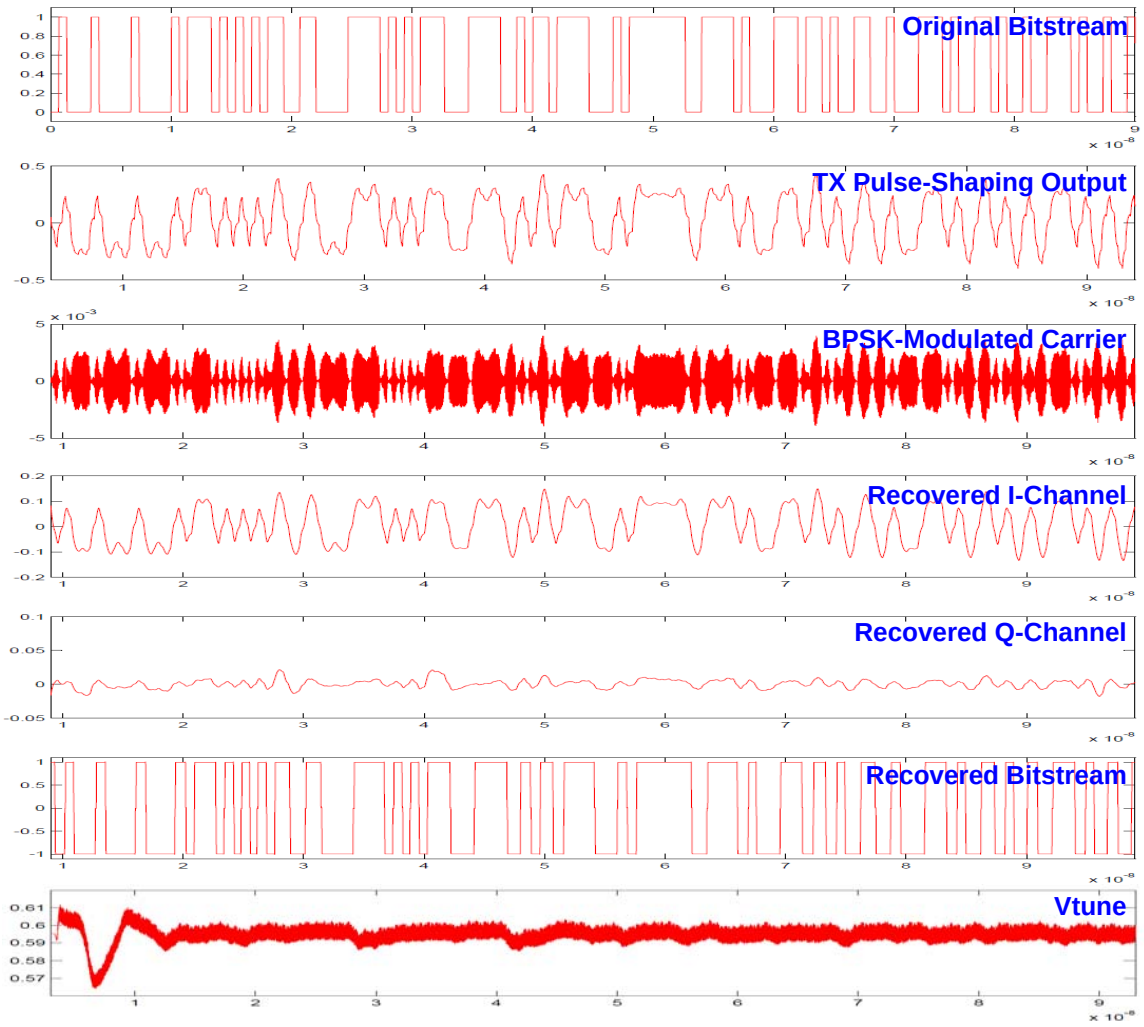


Figure 5-9: Cadence simulation results of the coherent BPSK demodulator with 35% raised-cosine pulse-shaped BPSK-modulated carrier

5.2.4 Circuit Implementation

In this section, circuits used in the ASP of the coherent BPSK-demodulator are discussed in more details. This includes the multiplier, error amplifier, loop filter and the QVCO buffer.

5.2.4.1 Multiplier

The error multiplier of Costas loop is based on the Gilbert-cell architecture and the circuit schematic is shown in Figure 5-10. The differential in-phase signal is fed to the Hi± and the quadrature-phase signal is fed to the LI±. The modified PMOS loading (transistors M7 and M8 and resistors R3 and R4) is used to reduce the potential DC offset at the output. The additional gain control through the switching transistors, M9 and M10, allows the multiplier to extend the dynamic range of BPSK-demodulation operation through either normal-gain or low-gain modes. The later is used for higher input power. The bleeding technique is applied in the multiplier to provide additional gain by funneling extra biasing current through resistors, R1 and R2, to transistors, M1 and M2. Table 5-1 shows the simulation performance of the multiplier.

Table 5-1: Simulation performance of the multiplier

Power Consumption	3.9 mW @ 1 V

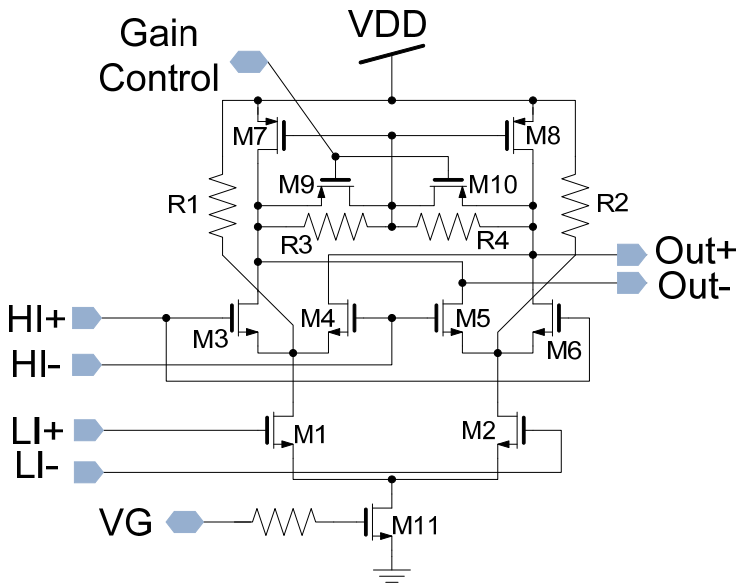


Figure 5-10: Circuit schematic of the multiplier / phase detector

DC transfer characteristic of the multiplier are shown in Figure 5-11, Figure 5-12 and Figure 5-13. Figure 5-11 shows the simulated differential output DC voltage versus the LI± differential input voltage (around the biasing point) of the multiplier at various fixed HI± voltages for the normal gain control setting. Figure 5-12 shows the same simulated differential output DC voltage plot for the low gain control setting. On the other hand, Figure 5-13 shows the simulated differential output DC voltage versus the HI± input voltage of the multiplier at different LI± voltages for the normal gain control setting. It should be noted that the multiplier behaves relatively linearly for input swings lower than ±200 mV and the gain control settings provides 2 dB switching between modes.

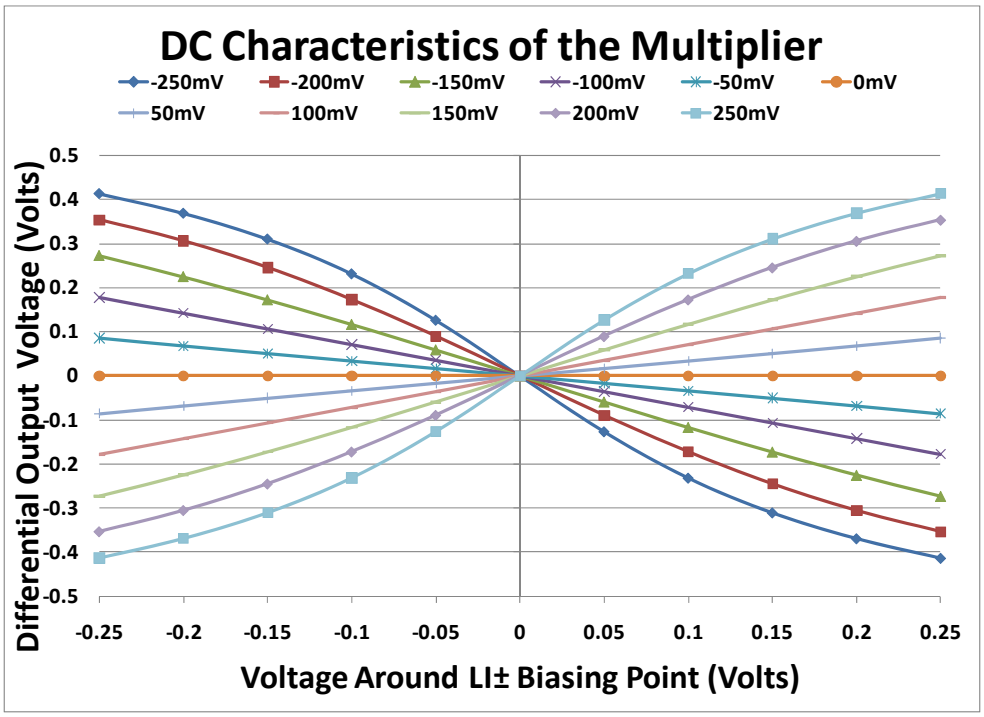


Figure 5-11: DC transfer characteristic of the multiplier: differential output versus LI± input for different fixed HI± voltages in the normal gain mode of the multiplier

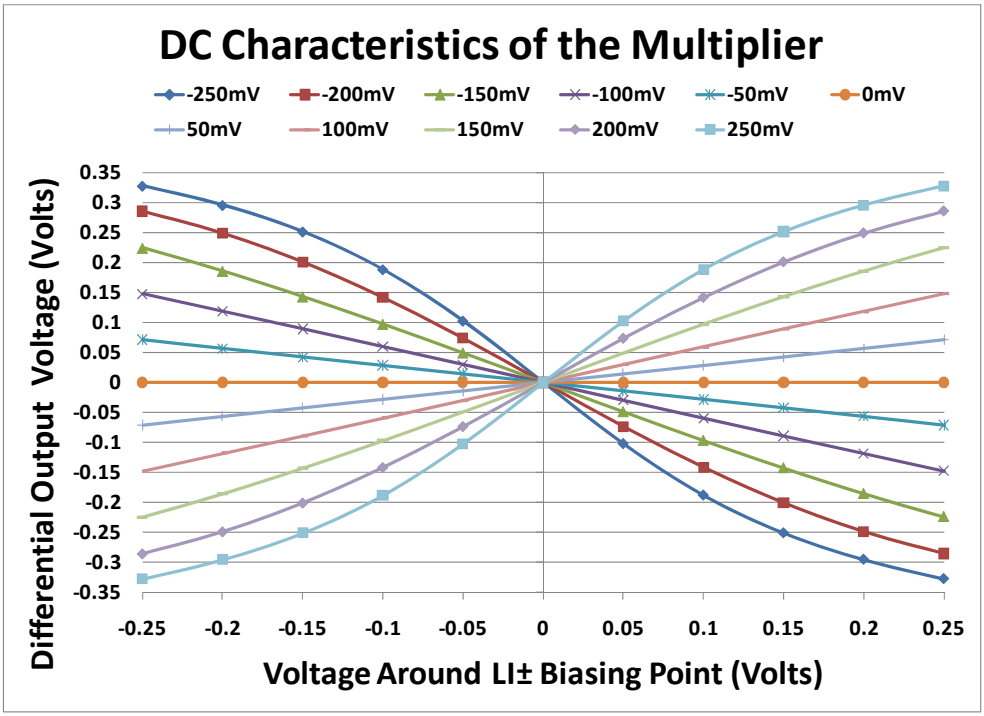


Figure 5-12: DC transfer characteristic of the multiplier: differential output versus LI± input for different fixed HI± voltages in the low gain mode of the multiplier

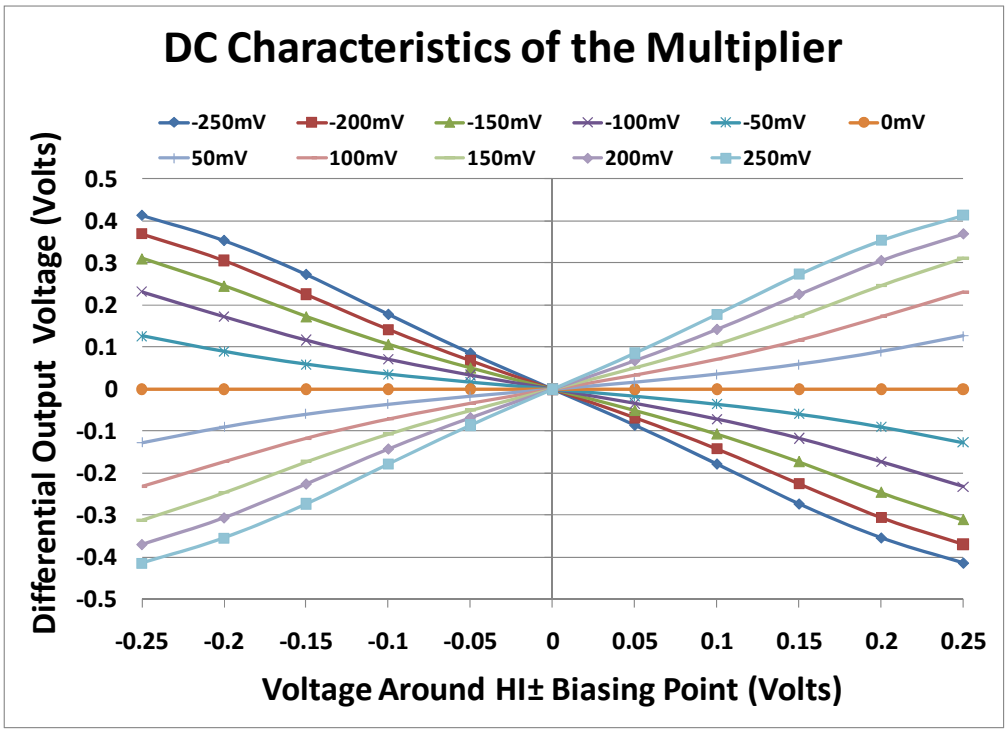


Figure 5-13: DC transfer characteristic of the multiplier: differential output versus HI± input for different fixed LI± voltages in the normal gain mode of the multiplier

5.2.4.2 ***Error Amplifier and Loop Filter***

The error amplifier (shown as the differential-pair in Figure 5-14) increases the overall loop gain of the Costas Loop. The loop filter consists of one pole and one zero, which are set by the combination of R_1, C_1 and C_2. The transfer function of the loop filter is expressed as

$$H(S) = \frac{1 + SC_1R_1}{1 + S(C_1 + C_2)R_1} \tag{20}$$

Additional gain-control can be achieved by varying the biasing voltage of the current sink. This is to increase the dynamic range of the BPSK demodulation operation when the incoming modulated signal power is large. The loop filter configuration can also be

changed (R_1 and C_2) through the serial-to-parallel interface (SPI). In contrast to the popular current-mode loop filter (with a charge-pump) in the PLL application, a voltage-mode loop filter is used instead. This decision is critical when the external tuning of the QVCO oscillation frequency is needed due to the process variations of the IC fabrication. Its importance is further manifested in the case of co-existence between the PLL and ASP, which is discussed in more details in Section 5.3.

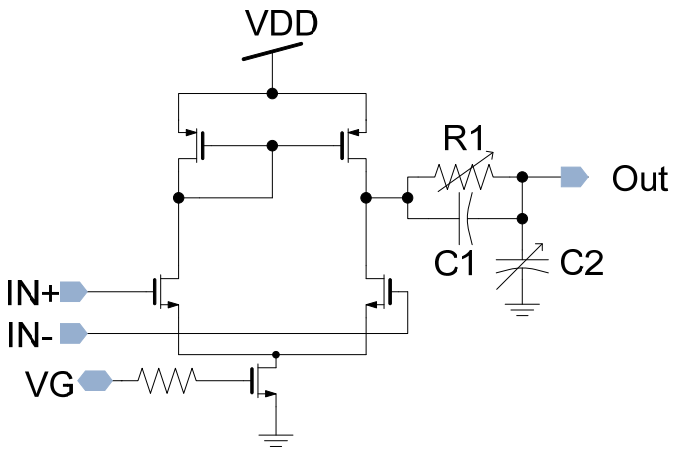


Figure 5-14: Circuit schematic of the error amplifier and loop filter

Figure 5-15 shows frequency responses of possible pole-zero configurations: the red line indicates the default loop response. Other frequency responses are shown as possible pole-zero combinations that could be selected through the SPI. As the input power of the BPSK-modulated carrier gets larger, the pole frequency needs be lower to keep the ASP stable by increasing the capacitor value, C_2, and/or the resistor value, R_1. Table 5-2 shows the simulation result of the error amplifier and loop filter.

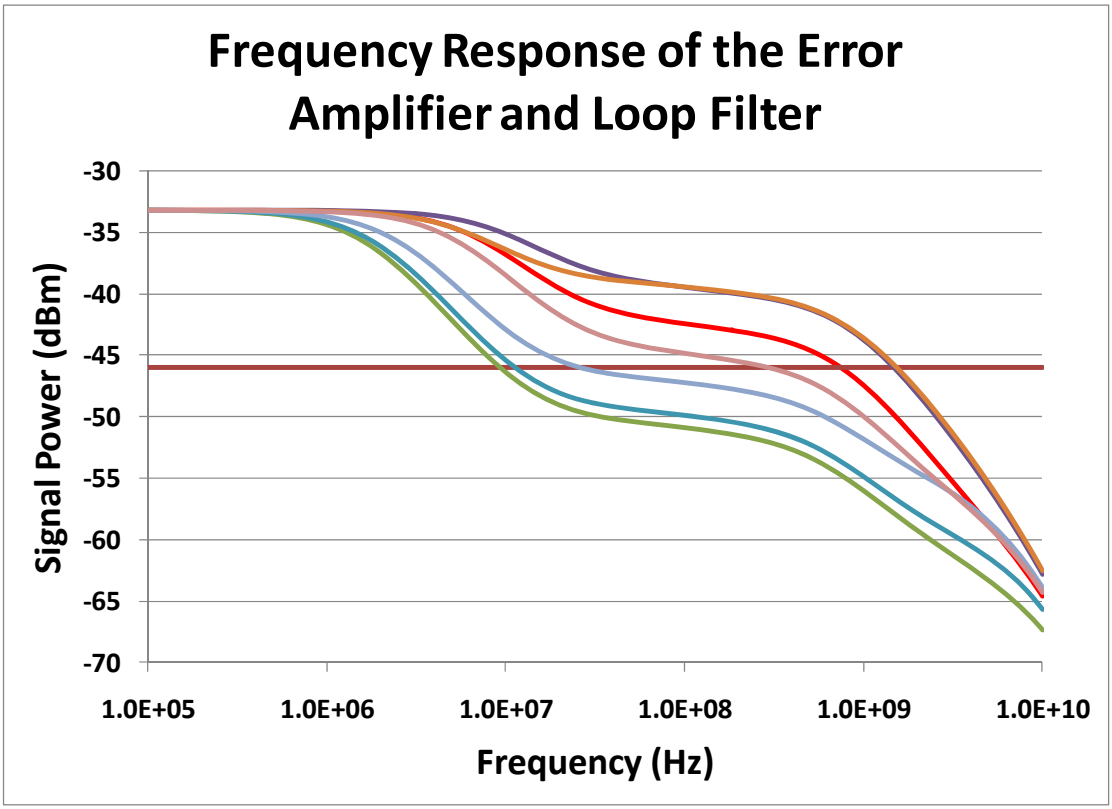


Figure 5-15: Frequency response of the voltage-mode loop filter for Costas loop

Table 5-2: Simulation performance of the error amplifier and loop filter

3-dB Cutoff Bandwidth	1.7 MHz
Gain (Single-Ended Output to Differential Inputs)	12.9 dB
Power Consumption	2.6 mW @ 1 V

5.2.4.3 QVCO Buffer

The main purpose of the QVCO buffer is to allow the output of the voltage-mode loop filter to be shifted to a proper DC level for the QVCO tuning port. When there is a significant frequency shift between the wireless transmitter and receiver LOs, which is larger than the frequency offset tolerance of the ASP, the external control can be used to

bring the two oscillation frequencies closer. Hence the ASP can maintain the frequency and phase synchronization. The schematic of the QVCO buffer is shown in Figure 5-16(a). The QVCO buffer architecture features a differential pair core with an input attenuator at each input. The differential pair implemented to provide sufficient output slew rate in order to drive the QVCO. Its gain is reduced as much as possible, since the buffer should, ideally, features 0 dB gain. This is essential for the QVCO buffer not to significantly alter the frequency characteristics in the sensitive feedback control loop for either the ASP or PLL operation. In order to reduce the overall buffer gain, an attenuator is introduced and the schematic is shown in Figure 5-16(b). The attenuators are implemented as complementary source follower buffers. The complementary architecture allows the input and output biasing voltages to be close.

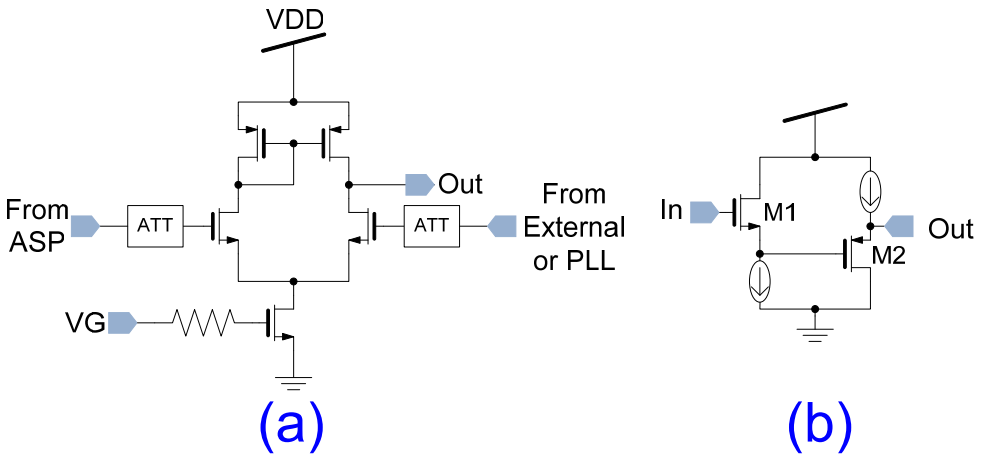


Figure 5-16: Circuit schematic of (a) the QVCO buffer; and (b) the attenuator

Figure 5-17 shows the DC transfer characteristic for one input of the QVCO buffer under different voltage settings of the other input. The black line indicates the desired DC point of the QVCO buffer, in which it provides an output DC range from 260 mV to 800 mV. With the measured K_{VCO}=2 GHz/Volt of the QVCO, this corresponds a

potential tuning of more than 1 GHz between the transmitter and receiver oscillator frequencies. Figure 5-18 depicts the frequency response of the QVCO from each input and it should be noted that the QVCO buffer provides little gain to either signal path. Table 5-3 shows the simulation performance of the QVCO buffer. Although the bandwidth of the QVCO buffer is 300MHz, this specification is irrelevant as the preceding loop filter has a much lower cut-off frequency around or below 10 MHz and it ultimately dominates the overall loop bandwidth of the ASP.

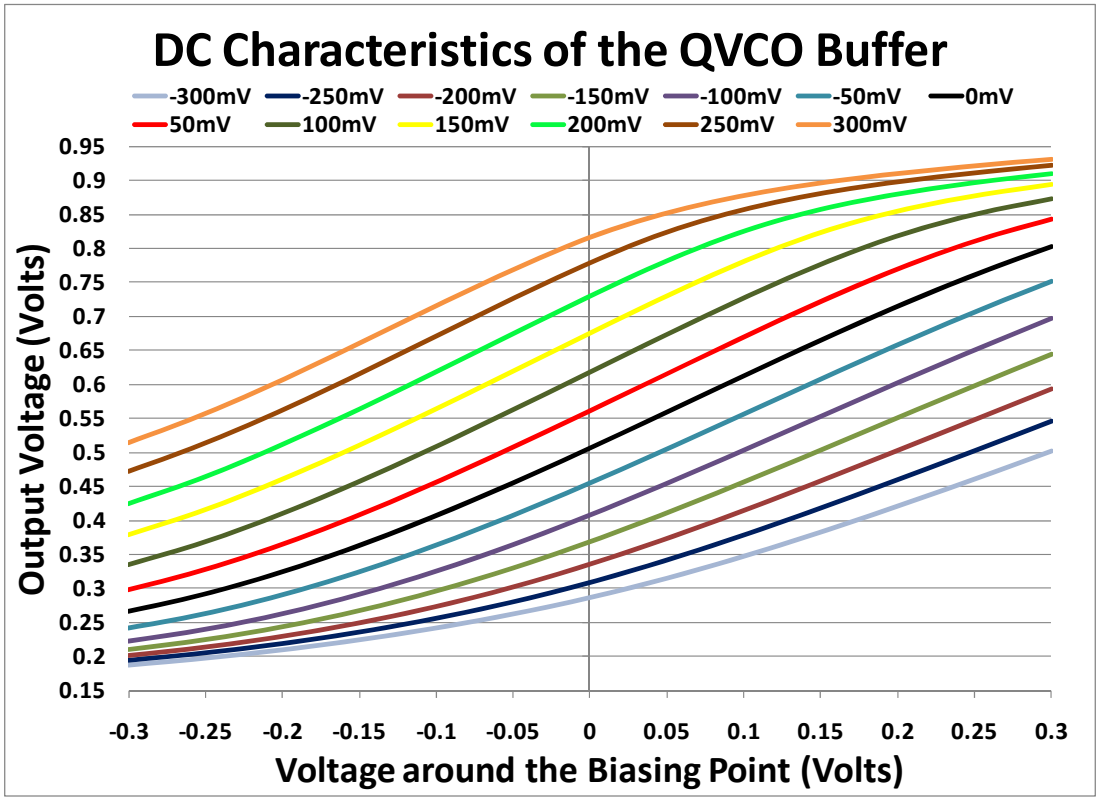


Figure 5-17: DC transfer characteristic of the QVCO buffer with sweeping DC input around the biasing point

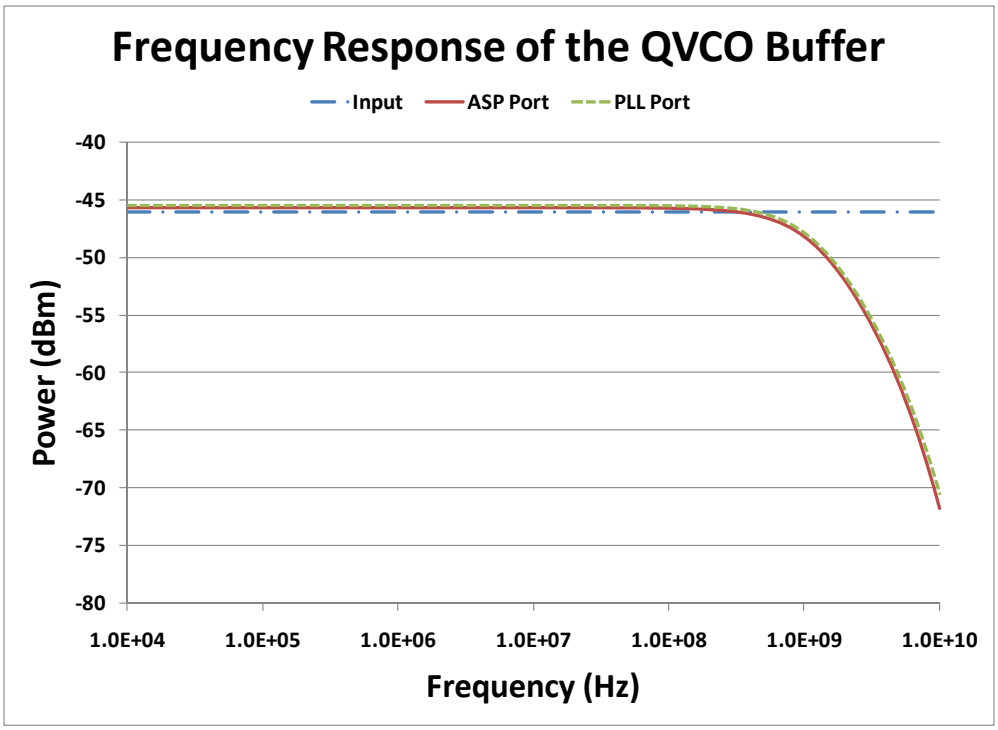


Figure 5-18: Frequency response of the QVCO buffer

Table 5-3: Simulation performance of the QVCO buffer

Bandwidth	300 MHz
Gain	0.5 dB
Power Consumption	3 mW @ 1 V

5.2.5 Measurement Setup

Figure 5-19 shows the micrograph of the analog quadrature front-end with the integrated ASP for coherent BPSK multi-gigabit demodulation. A photo of the test module is also shown. The overall size is 1.3 mm × 1.2 mm including all bonding pads. The chip is designed and fabricated using standard 90 nm CMOS process. As seen from Figure 5-19, the compact layout allows plenty of room for higher-level integration of

additional ADCs and DSPs if desired. The same BER measurement setup is used as in Section 4.2.3.

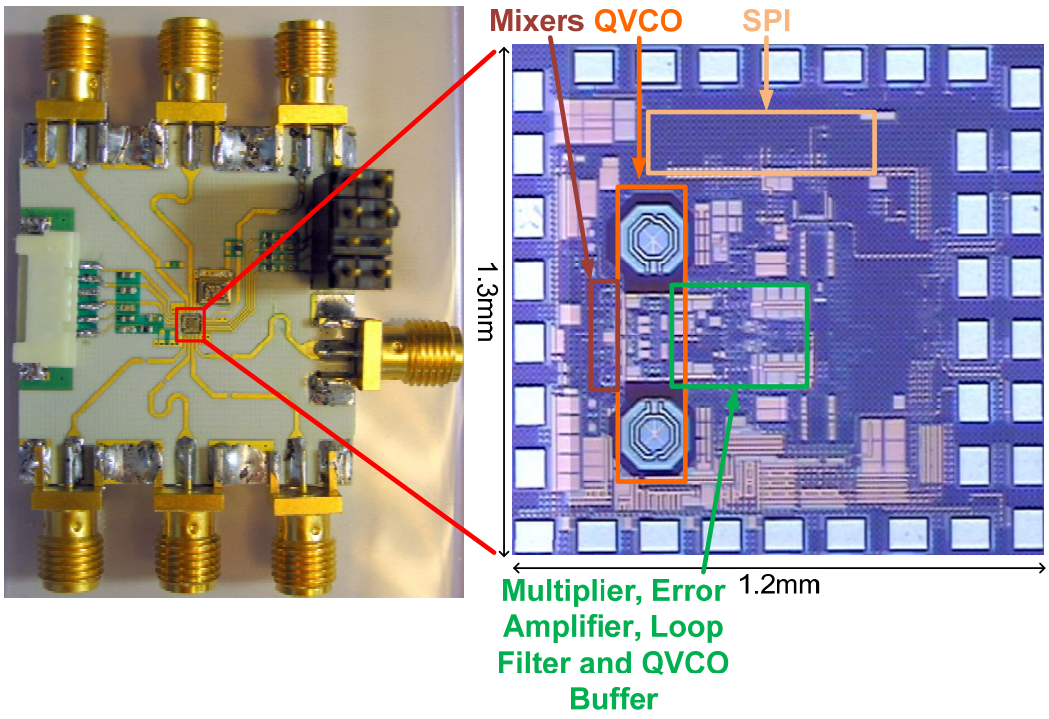
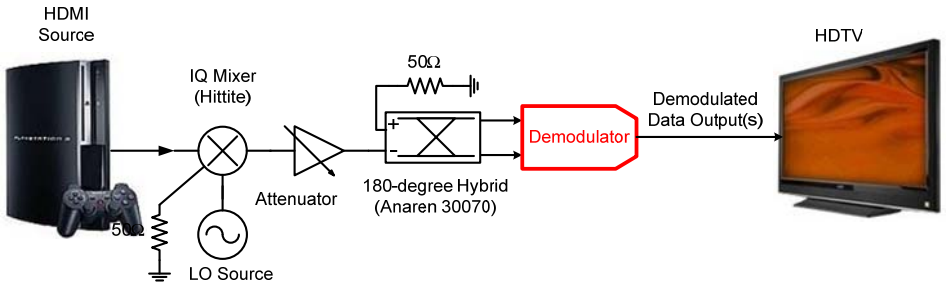
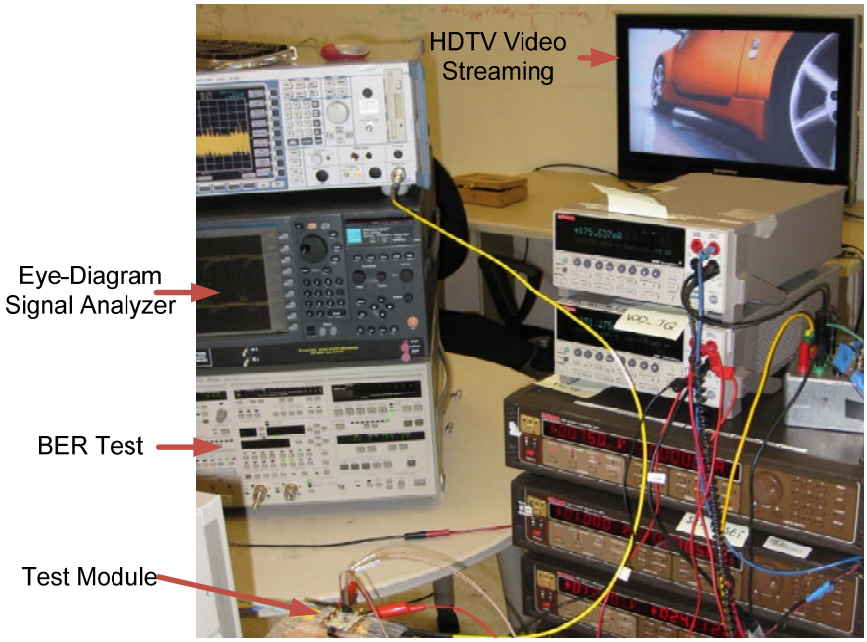


Figure 5-19: (right) Micrograph of the fabricated analog quadrature front-end with built-in coherent BPSK multi-gigabit demodulator; (left) test module used for measurement

Other than the standard BER measurement, a HD video streaming experiment is also performed to test the stability of the Costas loop and its setup is shown in Figure 5-20(a). A HDMI source is first serialized and the resulting bitstream modulates the carrier using the external mixer in the same manner as in the BER measurement setup. The coherent BPSK demodulator then recovers the original video content in the serial format, which is later converted back to a HDMI-compatible format. The HDMI source (i.e. XBOX360 in this case) and the HD TV are commercially available in local electronic stores. Figure 5-20(b) shows the photo of the actual HD streaming setup.



(a)



(b)

Figure 5-20: (a) Measurement setup of the HD video streaming; (b) photo of the actual setup

5.2.6 Performance Evaluation

Table 5-4 shows the measured and simulated performance summary of the coherent multi-gigabit BPSK demodulator. The total power consumption is 64.5 mW (including mixers, QVCO, PLL, amplifier, differential comparator, baseband amplifiers with AGC, and the ASP) from a single 1.0 V supply. However, only 7 mW out of the 64.5 mW is dedicated for BPSK demodulation (i.e. the ASP) as the rest of power

consumption comes from the normal operation of the analog quadrature front-end. In addition, the minimum sensitivity of the BPSK demodulator is about -47 dBm (at 1.728 GBps) and it increases slightly with rising data speed. A maximum raw speed of 3.5 Gbps has been demonstrated with automatic carrier phase and frequency synchronization. The synchronization range is more than ±100 MHz. The overall dynamic range of the multi-gigabit demodulator (44 dB) results from the dynamic range of the AGC, 23 dB, and that of the ASP itself, 21 dB.

Table 5-4: Performance summary of the coherent multi-gigabit BPSK demodulator

	Simulation	**Measurement**
Synchronization Range	±95 MHz	±105 MHz
Minimum Sensitivity	-49 dBm @ 2 Gbps	-47 dBm @ 1.728 Gbps
Dynamic Range	47 dB with AGC	44 dB with AGC
DC Power Consumption	64 mW @ 1 V	64.5 mW @ 1 V (only 7 mW is used for ASP)

At several data rates, the measured BER at various input power of the BPSK-modulated carrier is shown in Figure 5-21. The minimum sensitivities at data rates of 0.864 Gbps, 1.485 Gbps and 1.782 Gbps are limited by the inherent single-to-noise ratio with a deterministic system noise floor. At higher data rates, namely 2.5 Gbps and 2.9 Gbps, they are limited by the inherent baseband bandwidth of the analog quadrature front-end. The 3.5 Gbps data rate is made possible by enabling a high-bandwidth mode in the analog quadrature front-end, in which the baseband VGA gain is traded off for a higher cut-off frequency. Hence, the measured minimum sensitivity at 3.5 Gbps is much higher than others in the same BER plot. The measured eye-diagrams are shown in

Figure 5-22 for speeds at 0.864 Gbps, 1.485 Gbps, 1.782 Gbps, 2.5 Gbps, 2.9 Gbps and 3.5 Gbps.

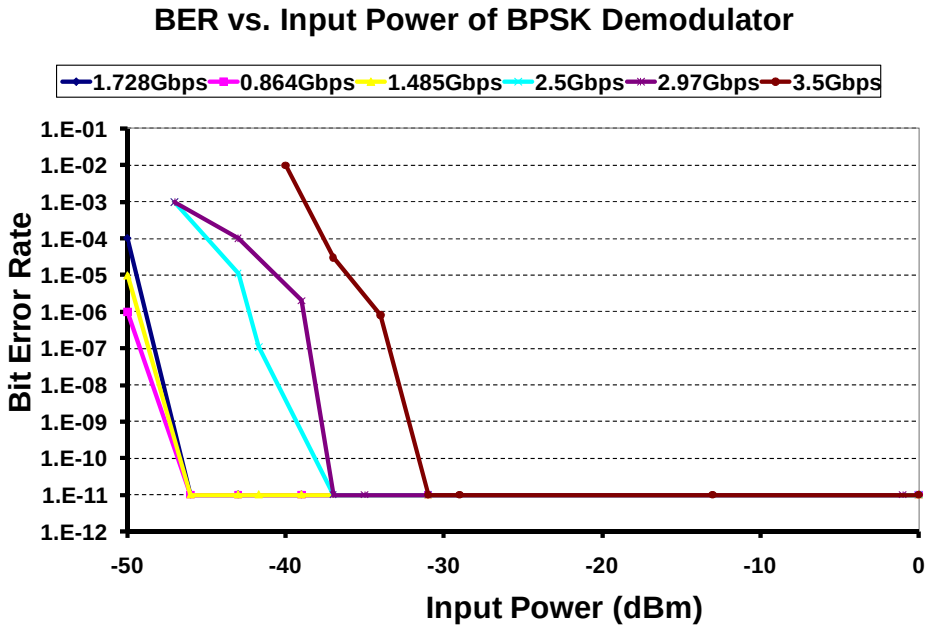


Figure 5-21: Measured BER at various input power of the BPSK-modulated IF carrier at 0.864 Gbps, 1.485 Gbps, 1.728 Gbps, 2.5 Gbps, 2.9 Gbps and 3.5 Gbps

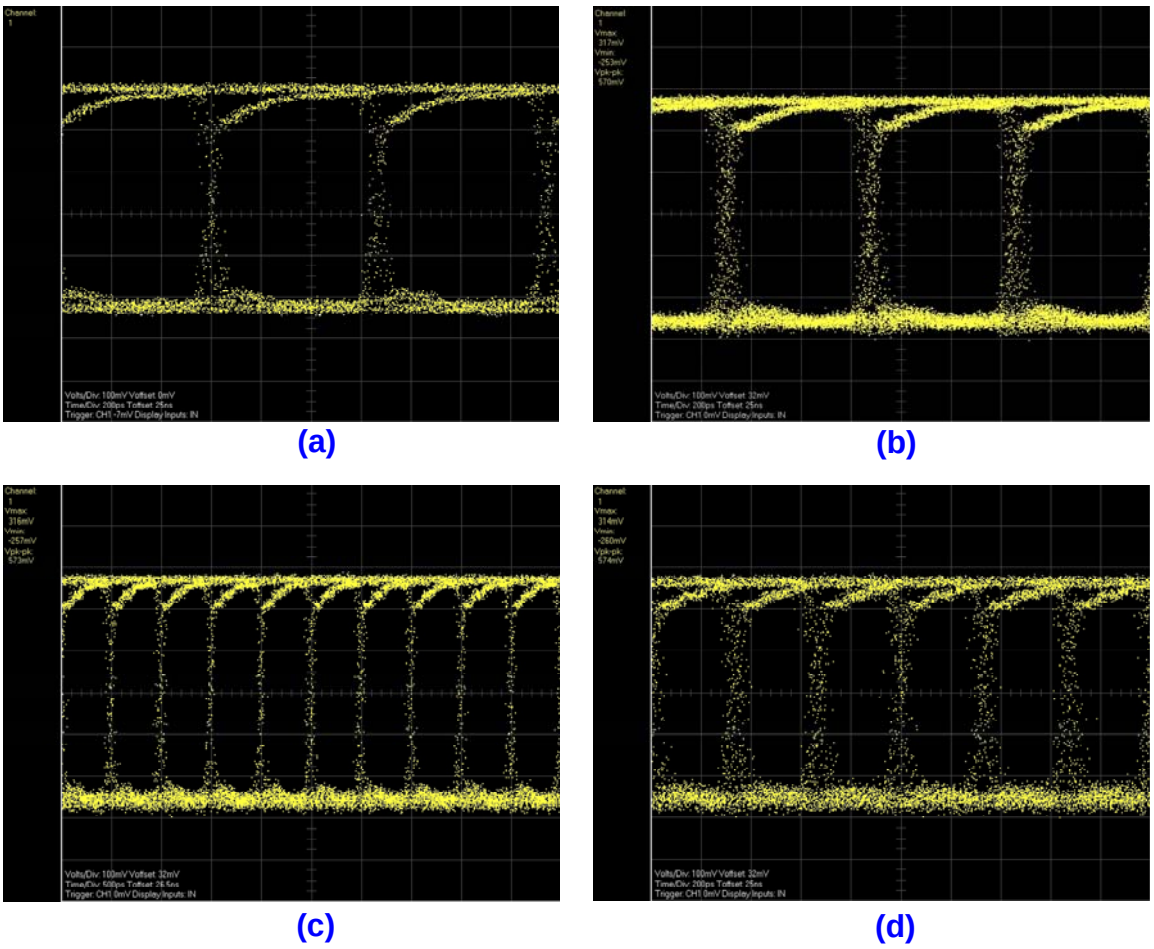


Figure 5-22: Measured eye-diagrams of the coherent BPSK demodulator: (a) IF=-43 dBm at 1.485 Gbps, error-free; (b) IF=-40 dBm at 1.728 Gbps, error-free; (c) IF=-35 dBm at 2 Gbps, error-free; and (d) IF=-30 dBm at 3.5 Gbps, BER=1E-9

5.3 Interaction of ASP and PLL

As mentioned earlier in Section 5.2, one drawback of the Costas loop is its frequency acquisition time. In order to reduce this acquisition time of the Coats loop, an integrated PLL is used first to bring the QVCO oscillation to the desired frequency before the ASP takes over of the remaining frequency and phase synchronization during the demodulation phase. Since both the ASP and PLL need to take control of the tuning port

of the QVCO, the QVCO buffer becomes an important interface between them. An architecture shown in Figure 5-23 is implemented for this purpose. In order to allow the ASP and PLL to control the QVCO separately but not simultaneously, the ASP and PLL is not operating at the same time. A detailed interfacing diagram is shown in Figure 5-24. During the initialization of the receiver, the PLL is first given the control of the QVCO to lock the oscillation frequency with an integer multiple (i.e. division of 480) of the external crystal reference. At this time, signal path switches, “SWA” and “SWC”, are ON and they allow the PLL tuning signal to adjust the QVCO frequency and the memory cell circuit to continuously sample the tuning signal. Once the receiver initialization is over, switches, “SWA” and “SWC”, are OFF and switch, “SWB”, is ON. This handover mechanism decouples the PLL control of the QVCO and utilizes the final settled PLL tuning voltage as a fixed DC value at the PLL-side input of the QVCO buffer. The ASP then takes over the control of QVCO for it synchronization operation as discussed in Section 5.2.

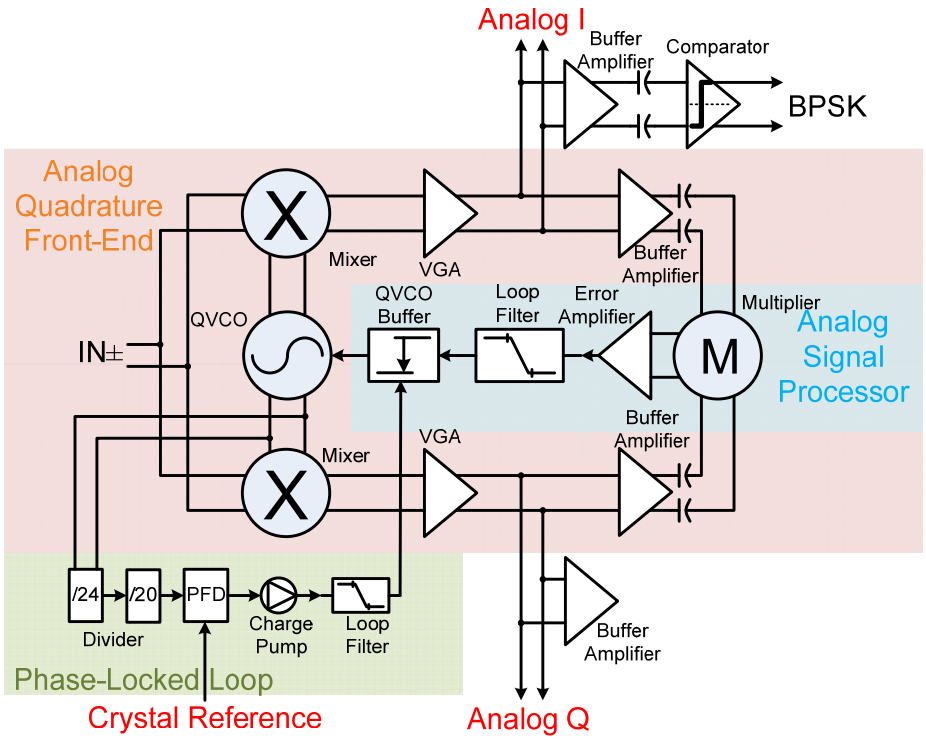


Figure 5-23: Architecture of the coherent BPSK demodulator with an integrated PLL

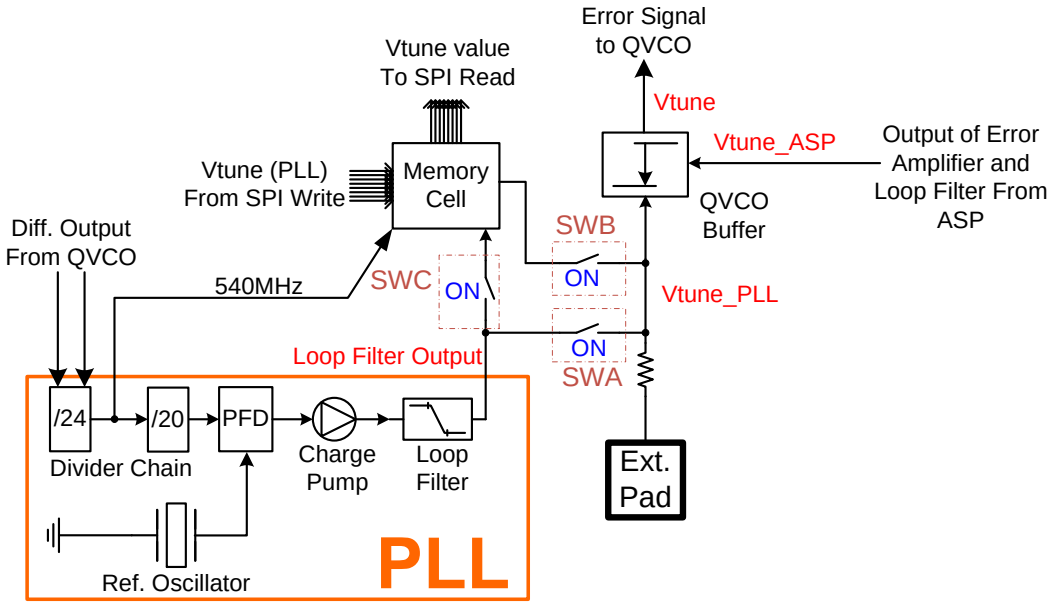


Figure 5-24: Detailed schematic of the ASP and PLL handover

5.3.1 Memory Circuit

The memory circuit functions as an ADC using a 540 MHz clock signal generated in the divider stage of the PLL. During the PLL operation period, the memory circuit samples the "Vtune_PLL" control voltage of the QVCO that comes from the PLL and "remembers" the value in an 8-bit memory cell. Once, the receiver is in the actual demodulation mode, the last sampled and stored "Vtune_PLL" voltage is applied at the PLL input of the QVCO buffer. This brings the QVCO operating frequency close to the incoming BPSK-modulated carrier. Hence the ASP can take over the carrier-phase synchronization and minor frequency tracking.

The detailed block diagram of the memory cell circuit is shown in Figure 5-25. The 540 MHz clock feeds directly to an 8-bit counter that goes from "00000000" to "11111111" repetitively. The 8-bit output connects directly to an 8-bit DAC, which covers the full scale (i.e. 0 V to 1 V) of the PLL tuning control voltage. As the output of the 8-bit DAC cycles through 0 V to 1 V, its voltage is being compared with the loop filter output from PLL. Every times the tuning control voltage is larger than the counter DAC output, the compactor triggers storing of the current 8-bit counter value into eight parallel D-flip-flops. This process continues until the PLL finally settles at a stable voltage value, which in turn locks the QVCO frequency to a desired point. Once this receiver initialization is complete, an external control signal, "Memory Sample", triggers the second set of 8-bit D-flip-flop to store the last 8-bit sampled DAC value. This value is then used to set another 8-bit DAC, which is of the same type as the one used in the counter output. The sampled DAC output is the final quantized sample of the settled PLL

tuning control voltage. One thing should be noted that the operation of the memory circuit does not consume any static current once the sample is retrieved. Hence it does not increase the overall power consumption of the ASP operation.

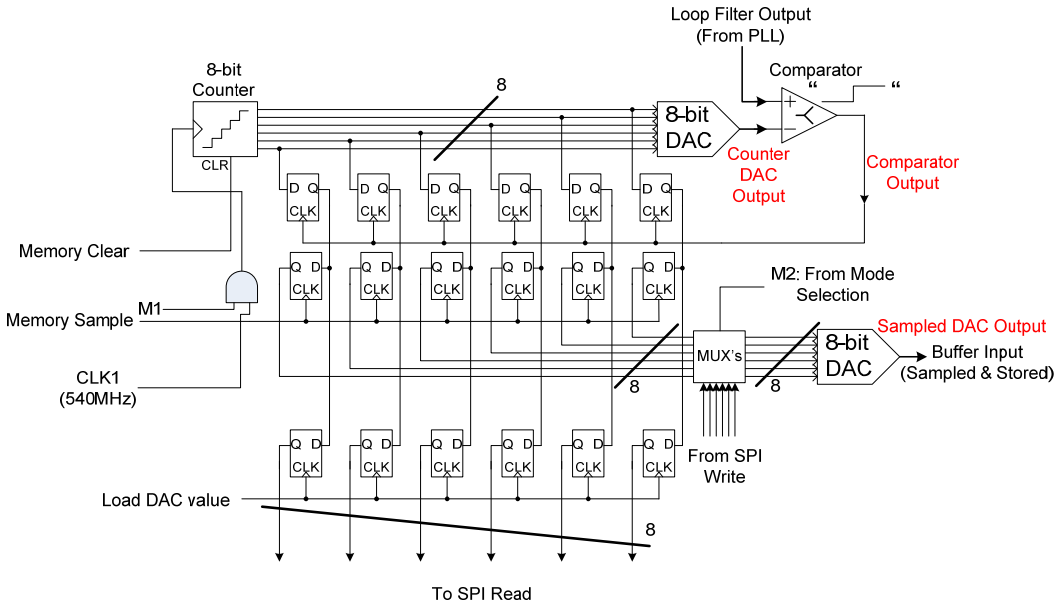


Figure 5-25: Block diagram of the memory circuit implemented in the ASP-PLL handover mechanism

5.3.2 Performance

Figure 5-26 shows the transient Cadence simulation results of the ASP-PLL handover mechanism. Please refer to Figure 5-24 and Figure 5-25 for the respective denoted waveforms, which are highlighted nodes in red. The PLL operation shown in Figure 5-26 takes approximately 1 µs (as shown by the "Loop Filter Output") to settle at its final value. During this time, The "Counter DAC Output" goes from 0 V to 1 V every $2^8/(540\times10^6)$=474 ns. Within each counter cycle, the "Comparator Output" is triggered once and the 8-bit counter value is stored simultaneously in to the eight D-flip-flops.

While the PLL has the control of the QVCO, the “Vtune” and “Vtune_PLL” waveforms closely tracks that of “Loop Filter Output”. After approximately 1.45 µs since the start-up of the PLL, assuming that the receiver system is ready to start demodulating the incoming carrier, switches “SWA” and “SWC” are OFF and the complementary “SWB” is ON. The “Sampled DAC Output” is set to the final settled PLL tuning voltage. This ASP and PLL handover mechanism is verified in the measurement and it has been proven to have no impact on the individual operation of either ASP or PLL.

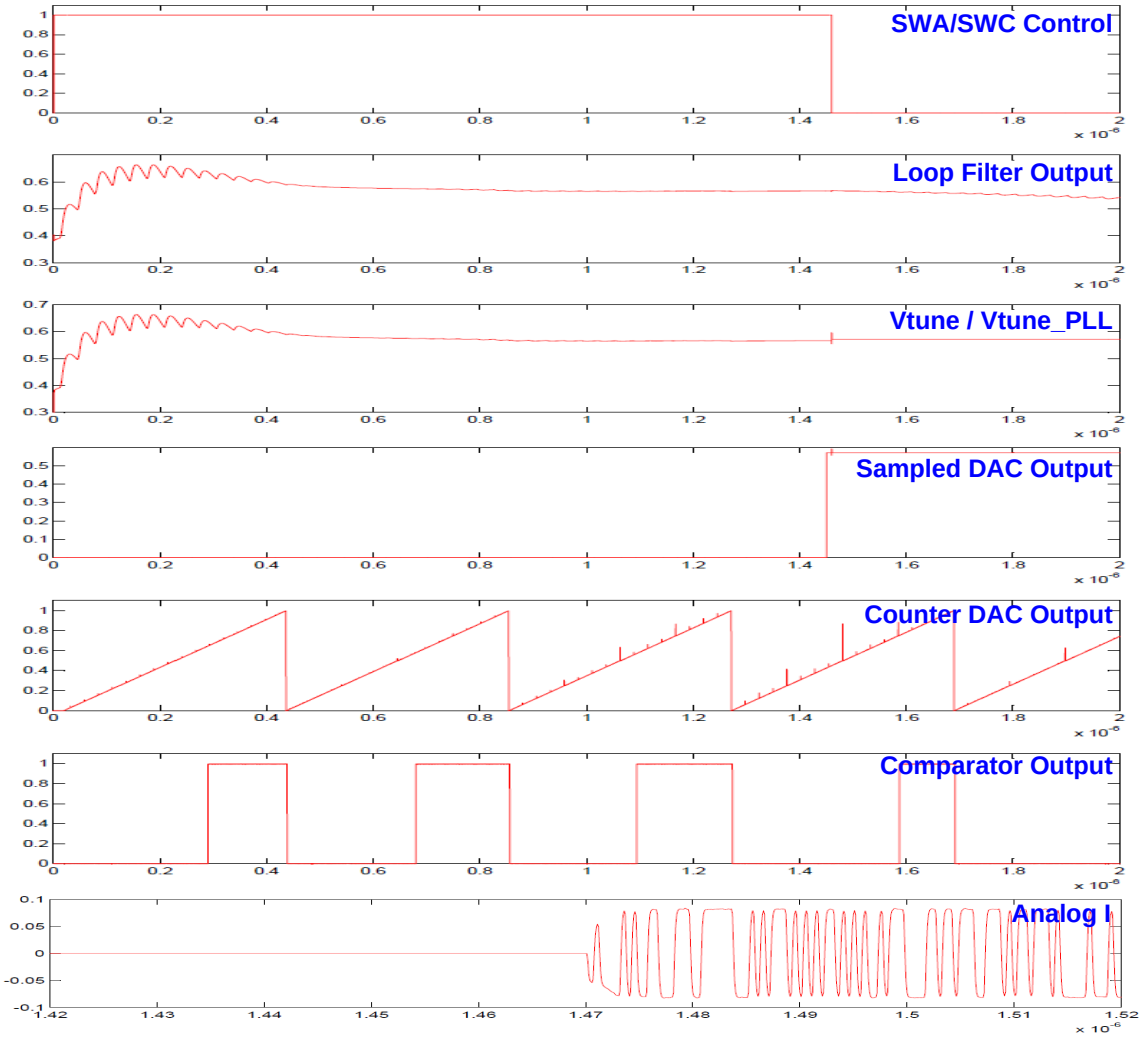


Figure 5-26: Transient simulation results of the ASP-PLL handover mechanism in Cadence environment

5.4 Summary

A robust coherent multi-gigabit BPSK demodulator is shown to achieve a maximum speed of 3.5 Gbps using the same analog quadrature front-end as shown in Section 3 with an integrated ASP based on the Costas loop architecture. With merely 7mW in addition to the power consumption of the analog quadrature front-end, the ASP achieves ultra-low power 2 pJ/bit efficiency. Furthermore, an innovative seamless handover mechanism between the ASP and PLL is designed and implemented to reduce the frequency acquisition time of the coherent demodulator. This demodulator design has been implemented and integrated in a 60 GHz wireless receiver. The system has been demonstrated in a product prototype to stream HD video as well as transfer large multi-media files at multi-gigabit speed.

Chapter VI

Conclusions

The final chapter concludes the research in developing multi-gigabit low-power low-cost wireless CMOS demodulator for the next-generation high-speed portable transceivers. A list of technical contributions from this work is presented. Potential research directions for future development related are also discussed.

6.1 Technical Contributions

The technical contributions of this research are:

- The potentials of implementing ultra-low power multi-gigabit demodulator are investigated for next-generation portable wireless applications in UWB and millimeter-wave frequencies. It is found that the traditional demodulator architecture involving power-hungry data-converters and high-speed DSP modems analog signal processor can be replaced by exploiting analog signal processor in deep sub-micron CMOS technologies. A maximum data transmission speed of 3.5 Gbps is achieved by the implemented 60 GHz integrated wireless transceiver.
- A fully-integrated analog quadrature front-end has been designed and fabricated in standard 90 nm CMOS technology using broadband techniques. It exhibits an

IF-to-baseband conversion gain of 25 dB with 1.8 GHz of baseband bandwidth and a dynamic range of 23 dB while consuming only 46 mW from a low voltage 1 V supply. Such analog front-end is compatible to the traditional digital demodulation architecture (ADC/DSP) with further integration possibilities. Further increase in bandwidth and reduction in power consumption can be made possible with the same circuit topologies when using advanced technologies such as 65 nm and 45 nm.

- Ultra-Low power 10.67 pJ/bit non-coherent ASK demodulator is designed and fabricated in 90nm CMOS. It is capable of a maximum speed of 3 Gbps with frequency offset tolerance of ±500 MHz while consuming 32 mV from 1.8 V supply. Such low-power design can be useful for wireless docking or time capsule applications when coverage distance is below one meter.

- Ultra-Low power 3 pJ/bit analog signal processor for non-coherent ASK demodulator is designed and fabricated in 90 nm CMOS. This I^2+Q^2 architecture utilizes the power detector circuitry inside the baseband AGC amplifiers of the analog quadrature front-end. With this compact design, it provides the analog quadrature front-end the capability of multi-gigabit demodulation without any significant impact on the power budget and the overall layout of the integrated system. The demodulator has been demonstrated to achieve a maximum data speed of 2.5 Gbps with frequency offset tolerance of ±500 MHz and a minimum sensitivity of -38 dBm. In addition, it can also be used as a DBPSK demodulator.

- Ultra-Low power 2 pJ/bit analog signal processor for coherent BPSK demodulator is designed and fabricated in 90 nm CMOS. The carrier-recovery mechanism is based on the Costas loop architecture, in which the analog quadrature front-end is employed with additional multiplier, error amplifier and loop filter. With this compact design, it provides the analog quadrature front-end the capability of multi-gigabit demodulation without any significant impact on the power budget and the overall layout of the integrated system. The demodulator has been demonstrated to achieve a maximum data speed of 3.5 Gbps with automatic phase and frequency tracking of ±105 MHz and a minimum sensitivity of -50 dBm.

- Innovative fast frequency-acquisition using PLL is integrated with the multi-gigabit demodulator. Seamless handover between the ASP and PLL is achieved through continuous sampling using analog voltage memory circuits. By combining the two operations, the PLL is given the control of the VCO during the start-up period (i.e. for the oscillation frequency of the VCO to lock onto the reference frequency) of the receiver then the ASP takes over the VCO to maintain the phase and minor frequency synchronization simultaneously. The issue of slow settling time in the Costas loop is alleviated with this PLL-ASP handover mechanism.

- The fully-integrated multi-mode multi-gigabit BPSK/ASK CMOS demodulator is implemented with the millimeter-wave front-end in the world-first low-power digital 60 GHz wireless radio. Wireless HD video streaming of 1.485 Gbps without FEC has been demonstrated using this radio transceiver. In addition,

high-speed wireless data transfer with a wide supported data transmission speeds from 500 Mbps up to 3.5 Gbps has also been verified with the same measurement setup.

6.2 Future Work

In the future, this research work can be extended into the following areas:

- Practical implementation of coherent QPSK using the same analog quadrature front-end: Based on the modified Costas loop architecture [44], multi-gigabit QPSK demodulator can be realized in the same fashion as the coherent BPSK demodulation technique demonstrated in this dissertation. However, the data transmission speed is doubled without incurring drastic change in the overall power consumption.
- Possible integration of matched filter in the baseband signal path: This could improve the minimum sensitivity and the synchronization locking range of the current BPSK demodulator by maximizing the signal-to-noise ratio in the presence of stochastic noise while the demodulator makes the (soft or hard) decision of digital "1" and "0".
- Optional integration of higher-order baseband filtering (e.g. beyond 2^{nd}-order Butterworth, Chebyshev Type I&II and elliptic filters): This feature can be helpful for improved anti-aliasing and noise-shaping in the traditional digital demodulation approaches as only the analog quadrature front-end is used.

- Application of the low-power multi-gigabit in a beam-forming phase-array system is recommended: The phase-array feature broadens the coverage of the current demodulator design into the NLOS environment. By means of using adaptive beam-forming phase-array system, the robustness of the multi-gigabit wireless transmission can be dramatically improved in the constantly varying wireless channel caused by an unpredictable clustered environment. The best direct or reflective wireless signal path is always chosen by the beam forming algorithm to maintain uninterrupted data transmission and avoid nulls in the desired direction.

- Cognitive radio and multi-band system incorporating the multi-gigabit demodulator: As more functions are integrated into the mobile devices, such as the Wi-Fi and Bluetooth capabilities inside the 3G (or even 4G) cellular phones, multi-gigabit data transfer can be the next technology candidate to be included in the next-generation mobile communication device. This requires the size and power consumption of the target wireless transceiver to be further reduced. With the integration of multi-band and multi-mode operations in one single device, wireless connectivity can be optimized, configured (or even switched in-between) in terms of the desired data speed (from several kbps of voice service to a few Gbps of data transfer) and its coverage (from several kilometers of cellular service to a few meters of WPAN). However, there are still issues and technical challenges to be addressed involving from the top protocol-level, the PHY-layer handler, antenna packaging to the actual system and circuit implementation before the cognitive and multi-mode radio to be realized.

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Vita

David A. Yeh was born in Taipei, Taiwan. He received the Bachelor of Engineering degree in Electrical and Electronic Engineering from University of Auckland, Auckland, New Zealand, in 2001 and the M.S. degree in Electrical and Computer Engineering from Georgia Institute of Technology, Atlanta, in 2004. He is currently pursuing his Ph.D. degree at Georgia Institute of Technology, where he is a member of the Microwave Application Group.

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